

HYS72D64301[G/H]BR-[5/6]-B

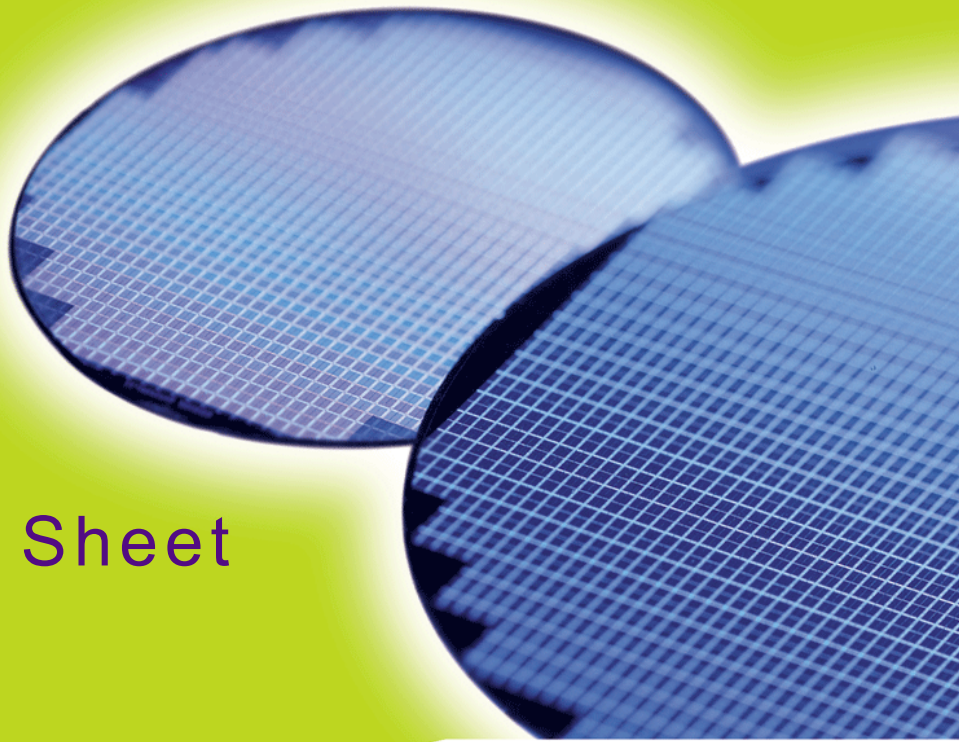
HYS72D128xxx[G/H]BR-[5/6/7]-B

HYS72D256220[G/H]BR-[5/6/7]-B

HYS72D256320[G/H]BR-[5/6/7]-B

*184 - Pin Registered Double-Data-Rate SDRAM Module
DDR SDRAM*

RoHS Compliant Products



Internet Data Sheet

Rev. 1.42



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | |
|--|--------------------------|
| HYS72D64301[G/H]BR-[5/6]-B, HYS72D128xxx[G/H]BR-[5/6/7]-B, HYS72D256220[G/H]BR-[5/6/7]-B, HYS72D256320[G/H]BR-[5/6/7]-B | |
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| All | Adapted internet edition |
| Previous Revision: 2006-03, Rev. 1.41 | |
| 67 | Editorial Change |
| Previous Revision: 2004-05, Rev. 1.4 | |

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1 Overview

1.1 Features

- 184-Pin Registered 8-Byte Dual-In-Line DDR SDRAM Module for “1U” PC, Workstation and Server main memory applications
- One rank 128M × 72 and 64M × 72 organization, and two ranks 256M × 72 organization
- Standard Double-Data-Rate Synchronous DRAMs (DDR SDRAM) with a single + 2.5 V (± 0.2 V) power supply and +2.6 V (± 0.1 V) power supply for DDR400
- Built with DDR SDRAMs in P-TFBGA-60 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- RAS-lockout supported $t_{RAP}=t_{RCD}$
- Re-drive for all input signals using register and PLL devices.
- Serial Presence Detect with E²PROM
- Low Profile Modules form factor: 133.35 mm × 28.58 mm (1.1”) × 4.00 mm and 133.35 mm × 30.48 mm (1.2”) × 4.00 mm
- Standard reference card layout Raw Card “A”, “B”, “C”, “D”.
- Gold plated contacts

TABLE 1
Performance

| Part Number Speed Code | | -5 | -6 | -7 | Unit | |
|------------------------|-----------|-------------|-------------|-------------|------|-----|
| Speed Grade | Component | DDR400B | DDR333B | DDR266A | — | |
| | Module | PC3200-3033 | PC2700-2533 | PC2100-2033 | — | |
| max. Clock Frequency | @CL3 | f_{CK3} | 200 | 166 | — | MHz |
| | @CL2.5 | $f_{CK2.5}$ | 166 | 166 | 143 | MHz |
| | @CL2 | f_{CK2} | 133 | 133 | 133 | MHz |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

1.2 Description

The HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B are low profile versions of the standard Registered DIMM modules with 1.1" inch (28.58) and 1.2" inch (30,40 mm) height for 1U Server Applications. The Low Profile DIMM versions are available as 64M × 72(512 MB), 128M × 72 (1 GB) and 256M × 72 (2 GB).

The memory array is designed with Double Data Rate Synchronous DRAMs for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. A variety of de coupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E²PROM device using the 2-pin I²C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

TABLE 2
Ordering Information for Lead - Containing Products

| Product Type ¹⁾ | Compliance Code ²⁾ | Description | SDRAM Technology |
|----------------------------|-------------------------------|----------------------------------|------------------|
| PC3200 (CL=3) | | | |
| HYS72D64301GBR-5-B | PC2700R-30331-A0 | one rank 512 MByte Reg. ECC DIMM | 512 MBit (×8) |
| HYS72D128300GBR-5-B | PC3200R-30331-C0 | one rank 1 GByte Reg. ECC DIMM | 512 MBit (×4) |
| HYS72D128321GBR-5-B | PC3200R-30331-B0 | two ranks 1 GByte Reg. ECC DIMM | 512 MBit (×8) |
| HYS72D256220GBR-5-B | PC3200R-30331-D0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (×4) |
| PC2700 (CL=2.5) | | | |
| HYS72D64301GBR-6-B | PC2700R-25330-A0 | one rank 512 MByte Reg. ECC DIMM | 512 MBit (×4) |
| HYS72D128300GBR-6-B | PC2700R-25330-C0 | one rank 1 GByte Reg. ECC DIMM | 512 MBit (×4) |
| HYS72D128321GBR-6-B | PC2700R-25330-B0 | two ranks 1 GByte Reg. ECC DIMM | 512 MBit (×8) |
| HYS72D256320GBR-6-B | PC2700R-25330-D0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (×4) |
| HYS72D256220GBR-6-B | PC2700R-25330-D0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (×4) |
| PC2100 (CL=2) | | | |
| HYS72D128300GBR-7-B | PC2100R-20330-C0 | one rank 1 GByte Reg. ECC DIMM | 512 MBit (×4) |
| HYS72D128321GBR-7-B | PC2100R-20330-B0 | two ranks 1 GByte Reg. ECC DIMM | 512 MBit (×8) |
| HYS72D256220GBR-7-B | PC2100R-20330-D0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (×4) |
| HYS72D256320GBR-7-B | PC2100R-20330-D0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (×4) |

- 1) All product types end with a place code designating the silicon-die revision. Reference information available on request.
Example: HYS72D128300GBR-5-B, indicating Rev.B die are used for SDRAM components.
- 2) The Compliance Code is printed on the module labels and describes the speed sort (for example "PC2100R"), the latencies (for example "20330" means CAS latency of 2.0 clocks, Row-Column-Delay (RCD) latency of 3 clocks and Row Pre-charge latency of 3 clocks), JEDEC SPD code definition version 0, and the Raw Card used for this module.



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

green
Product

TABLE 3**Ordering information for Lead - Free (RoHS Compliant) Products**

| Product Type ¹⁾²⁾ | Compliance Code ³⁾ | Description | SDRAM Technology |
|------------------------------|-------------------------------|----------------------------------|------------------|
| PC3200 (CL=3) | | | |
| HYS72D64301HBR-5-B | PC3200R-30331-A0 | one rank 512 MByte Reg. ECC DIMM | 512 MBit (x8) |
| HYS72D128300HBR-5-B | PC3200R-30331-C0 | one rank 1 GByte Reg. ECC DIMM | 512 MBit (x4) |
| HYS72D128321HBR-5-B | PC3200R-30331-B0 | two ranks 1 GByte Reg. ECC DIMM | 512 MBit (x8) |
| HYS72D256220HBR-5-B | PC3200R-30331-D0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (x4) |
| HYS72D256320HBR-5-B | PC3200R-30331-F0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (x4) |
| PC2700 (CL=2.5) | | | |
| HYS72D64301HBR-6-B | PC2700R-25330-A0 | one rank 512 MByte Reg. ECC DIMM | 512 MBit (x8) |
| HYS72D128300HBR-6-B | PC2700R-25330-C0 | one rank 1 GByte Reg. ECC DIMM | 512 MBit (x4) |
| HYS72D128321HBR-6-B | PC2700R-25330-B0 | two ranks 1 GByte Reg. ECC DIMM | 512 MBit (x8) |
| HYS72D256220HBR-6-B | PC2700R-25330-D0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (x4) |
| HYS72D256320HBR-6-B | PC2700R-25330-F0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (x4) |
| PC2100 (CL=2) | | | |
| HYS72D128300HBR-7-B | PC2100R-20330-C0 | one rank 1 GByte Reg. ECC DIMM | 512 MBit (x4) |
| HYS72D128321HBR-7-B | PC2100R-20330-B0 | two ranks 1 GByte Reg. ECC DIMM | 512 MBit (x8) |
| HYS72D256220HBR-7-B | PC2100R-20330-D0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (x4) |
| HYS72D256320HBR-7-B | PC2100R-20330-F0 | two ranks 2 GByte Reg. ECC DIMM | 512 MBit (x4) |

- 1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.
- 2) All product types end with a place code designating the silicon-die revision. Reference information available on request.
Example: HYS72D128300GBR-5-B, indicating Rev.B die are used for SDRAM components.
- 3) The Compliance Code is printed on the module labels and describes the speed sort (for example "PC2100R"), the latencies (for example "20330" means CAS latency of 2.0 clocks, Row-Column-Delay (RCD) latency of 3 clocks and Row Pre-charge latency of 3 clocks), JEDEC SPD code definition version 0, and the Raw Card used for this module.



2 Pin Configuration

The pin configuration of the Registered DDR SDRAM DIMM is listed by function in **Table 4** (184 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 5** and **Table 6** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 4
Pin Configuration of RDIMM

| Pin# | Name | Pin Type | Buffer Type | Function |
|------------------------|---------------------------|----------|-------------|---|
| Clock Signals | | | | |
| 137 | CK0 | I | SSTL | Clock Signal |
| 138 | $\overline{\text{CK0}}$ | I | SSTL | Complement Clock |
| 21 | CKE0 | I | SSTL | Clock Enable Rank 0 |
| 111 | CKE1 | I | SSTL | Clock Enable Rank 1 <i>Note: 2-rank module</i> |
| | NC | NC | SSTL | <i>Note: 1-rank module</i> |
| Control Signals | | | | |
| 157 | $\overline{\text{S0}}$ | I | SSTL | Chip Select of Rank 0 |
| 158 | $\overline{\text{S1}}$ | I | SSTL | Chip Select of Rank 1 <i>Note: 2-ranks module</i> |
| | NC | NC | — | <i>Note: 1-rank module</i> |
| 154 | $\overline{\text{RAS}}$ | I | SSTL | Row Address Strobe |
| 65 | $\overline{\text{CAS}}$ | I | SSTL | Column Address Strobe |
| 63 | $\overline{\text{WE}}$ | I | SSTL | Write Enable |
| 10 | $\overline{\text{RESET}}$ | I | LV-CMOS | Register Reset |
| Address Signals | | | | |
| 59 | BA0 | I | SSTL | Bank Address Bus 1:0 |
| 52 | BA1 | I | SSTL | |
| 48 | A0 | I | SSTL | Address Bus 11:0 |
| 43 | A1 | I | SSTL | |
| 41 | A2 | I | SSTL | |
| 130 | A3 | I | SSTL | |
| 37 | A4 | I | SSTL | |
| 32 | A5 | I | SSTL | |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Pin# | Name | Pin Type | Buffer Type | Function |
|---------------------|------|----------|-------------|--|
| 125 | A6 | I | SSTL | Address Bus 11:0 |
| 29 | A7 | I | SSTL | |
| 122 | A8 | I | SSTL | |
| 27 | A9 | I | SSTL | |
| 141 | A10 | I | SSTL | |
| | AP | I | SSTL | |
| 118 | A11 | I | SSTL | |
| 115 | A12 | I | SSTL | Address Signal 12 <i>Note: Module based on 256 Mbit or larger dies</i> |
| | NC | NC | — | <i>Note: 128 Mbit based module</i> |
| 167 | A13 | I | SSTL | Address Signal 13 <i>Note: 1 Gbit based module</i> |
| | NC | NC | — | <i>Note: Module based on 512 Mbit or smaller dies</i> |
| Data Signals | | | | |
| 2 | DQ0 | I/O | SSTL | Data Bus 63:0 |
| 4 | DQ1 | I/O | SSTL | |
| 6 | DQ2 | I/O | SSTL | |
| 8 | DQ3 | I/O | SSTL | |
| 94 | DQ4 | I/O | SSTL | |
| 95 | DQ5 | I/O | SSTL | |
| 98 | DQ6 | I/O | SSTL | |
| 99 | DQ7 | I/O | SSTL | |
| 12 | DQ8 | I/O | SSTL | |
| 13 | DQ9 | I/O | SSTL | |
| 19 | DQ10 | I/O | SSTL | |
| 20 | DQ11 | I/O | SSTL | |
| 105 | DQ12 | I/O | SSTL | |
| 106 | DQ13 | I/O | SSTL | |
| 109 | DQ14 | I/O | SSTL | |
| 110 | DQ15 | I/O | SSTL | |
| 23 | DQ16 | I/O | SSTL | |
| 24 | DQ17 | I/O | SSTL | |
| 28 | DQ18 | I/O | SSTL | |
| 31 | DQ19 | I/O | SSTL | |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Pin# | Name | Pin Type | Buffer Type | Function |
|------|------|----------|-------------|----------------------|
| 114 | DQ20 | I/O | SSTL | Data Bus 63:0 |
| 117 | DQ21 | I/O | SSTL | |
| 121 | DQ22 | I/O | SSTL | |
| 123 | DQ23 | I/O | SSTL | |
| 33 | DQ24 | I/O | SSTL | |
| 35 | DQ25 | I/O | SSTL | |
| 39 | DQ26 | I/O | SSTL | |
| 40 | DQ27 | I/O | SSTL | |
| 126 | DQ28 | I/O | SSTL | |
| 127 | DQ29 | I/O | SSTL | |
| 131 | DQ30 | I/O | SSTL | |
| 133 | DQ31 | I/O | SSTL | |
| 53 | DQ32 | I/O | SSTL | |
| 55 | DQ33 | I/O | SSTL | |
| 57 | DQ34 | I/O | SSTL | |
| 60 | DQ35 | I/O | SSTL | |
| 146 | DQ36 | I/O | SSTL | |
| 147 | DQ37 | I/O | SSTL | |
| 150 | DQ38 | I/O | SSTL | |
| 151 | DQ39 | I/O | SSTL | |
| 61 | DQ40 | I/O | SSTL | |
| 64 | DQ41 | I/O | SSTL | |
| 68 | DQ42 | I/O | SSTL | |
| 69 | DQ43 | I/O | SSTL | |
| 153 | DQ44 | I/O | SSTL | |
| 155 | DQ45 | I/O | SSTL | |
| 161 | DQ46 | I/O | SSTL | |
| 162 | DQ47 | I/O | SSTL | |
| 72 | DQ48 | I/O | SSTL | |
| 73 | DQ49 | I/O | SSTL | |
| 79 | DQ50 | I/O | SSTL | |
| 80 | DQ51 | I/O | SSTL | |
| 165 | DQ52 | I/O | SSTL | |
| 166 | DQ53 | I/O | SSTL | |
| 170 | DQ54 | I/O | SSTL | |
| 171 | DQ55 | I/O | SSTL | |
| 83 | DQ56 | I/O | SSTL | |
| 84 | DQ57 | I/O | SSTL | |
| 87 | DQ58 | I/O | SSTL | |
| 88 | DQ59 | I/O | SSTL | |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Pin# | Name | Pin Type | Buffer Type | Function |
|------|-------|----------|-------------|---|
| 174 | DQ60 | I/O | SSTL | Data Bus 63:0 |
| 175 | DQ61 | I/O | SSTL | |
| 178 | DQ62 | I/O | SSTL | |
| 179 | DQ63 | I/O | SSTL | |
| 44 | CB0 | I/O | SSTL | Check Bits 7:0 |
| 45 | CB1 | I/O | SSTL | |
| 49 | CB2 | I/O | SSTL | |
| 51 | CB3 | I/O | SSTL | |
| 134 | CB4 | I/O | SSTL | |
| 135 | CB5 | I/O | SSTL | |
| 142 | CB6 | I/O | SSTL | |
| 144 | CB7 | I/O | SSTL | |
| 5 | DQS0 | I/O | SSTL | Data Strobes 8:0 |
| 14 | DQS1 | I/O | SSTL | |
| 25 | DQS2 | I/O | SSTL | |
| 36 | DQS3 | I/O | SSTL | |
| 56 | DQS4 | I/O | SSTL | |
| 67 | DQS5 | I/O | SSTL | |
| 78 | DQS6 | I/O | SSTL | Data Strobes 8:0 |
| 86 | DQS7 | I/O | SSTL | |
| 47 | DQS8 | I/O | SSTL | |
| 97 | DM0 | I | SSTL | Data Mask 0 <i>Note: ×8 based module</i> |
| | DQS9 | I/O | SSTL | Data Strobe 9 <i>Note: ×4 based module</i> |
| 107 | DM1 | I | SSTL | Data Mask 1 <i>Note: ×8 based module</i> |
| | DQS10 | I/O | SSTL | Data Strobe 10 <i>Note: ×4 based module</i> |
| 119 | DM2 | I | SSTL | Data Mask 2 <i>Note: ×8 based module</i> |
| | DQS11 | I/O | SSTL | Data Strobe 11 <i>Note: ×4 based module</i> |
| 129 | DM3 | I | SSTL | Data Mask 3 <i>Note: ×8 based module</i> |
| | DQS12 | I/O | SSTL | Data Strobe 12 <i>Note: ×4 based module</i> |
| 149 | DM4 | I | SSTL | Data Mask 4 <i>Note: ×8 based module</i> |
| | DQS13 | I/O | SSTL | Data Strobe 13 <i>Note: ×4 based module</i> |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Pin# | Name | Pin Type | Buffer Type | Function |
|--|-------------|----------|-------------|---|
| 159 | DM5 | I | SSTL | Data Mask 5 <i>Note: x8 based module</i> |
| | DQS14 | I/O | SSTL | Data Strobe 14 <i>Note: x4 based module</i> |
| 169 | DM6 | I | SSTL | Data Mask 6 <i>Note: x8 based module</i> |
| | DQS15 | I/O | SSTL | Data Strobe 15 <i>Note: x4 based module</i> |
| 177 | DM7 | I | SSTL | Data Mask 7 <i>Note: x8 based module</i> |
| | DQS16 | I/O | SSTL | Data Strobe 16 <i>Note: x4 based module</i> |
| 140 | DM8 | I | SSTL | Data Mask 8 <i>Note: x8 based module</i> |
| | DQS17 | I/O | SSTL | Data Strobe 17 <i>Note: x4 based module</i> |
| EEPROM | | | | |
| 92 | SCL | I | CMOS | Serial Bus Clock |
| 91 | SDA | I/O | OD | Serial Bus Data |
| 181 | SA0 | I | CMOS | Slave Address Select Bus 2:0 |
| 182 | SA1 | I | CMOS | |
| 183 | SA2 | I | CMOS | |
| Power Supplies | | | | |
| 1 | V_{REF} | AI | — | I/O Reference Voltage |
| 184 | V_{DDSPD} | PWR | — | EEPROM Power Supply |
| 15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180 | V_{DDQ} | PWR | — | I/O Driver Power Supply |
| 7, 38, 46, 70, 85, 108, 120, 148, 168 | V_{DD} | PWR | — | Power Supply |
| 3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176 | V_{SS} | GND | — | Ground Plane |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Pin# | Name | Pin Type | Buffer Type | Function |
|---|-------------------|----------|-------------|--------------------------------|
| Other Pins | | | | |
| 82 | V _{DDID} | O | OD | V _{DD} Identification |
| 9, 16, 17, 71, 75, 76, 90, 101, 102, 103, 113, 163, 173 | NC | NC | — | Not connected |

TABLE 5
Abbreviations for Pin Type

| Abbreviation | Description |
|--------------|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NU | Not Usable (JEDEC Standard) |
| NC | Not Connected (JEDEC Standard) |

TABLE 6
Abbreviations for Buffer Type

| Abbreviation | Description |
|--------------|---|
| SSTL | Serial Stub Terminated Logic (SSTL2) |
| LV-CMOS | Low Voltage CMOS |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. |

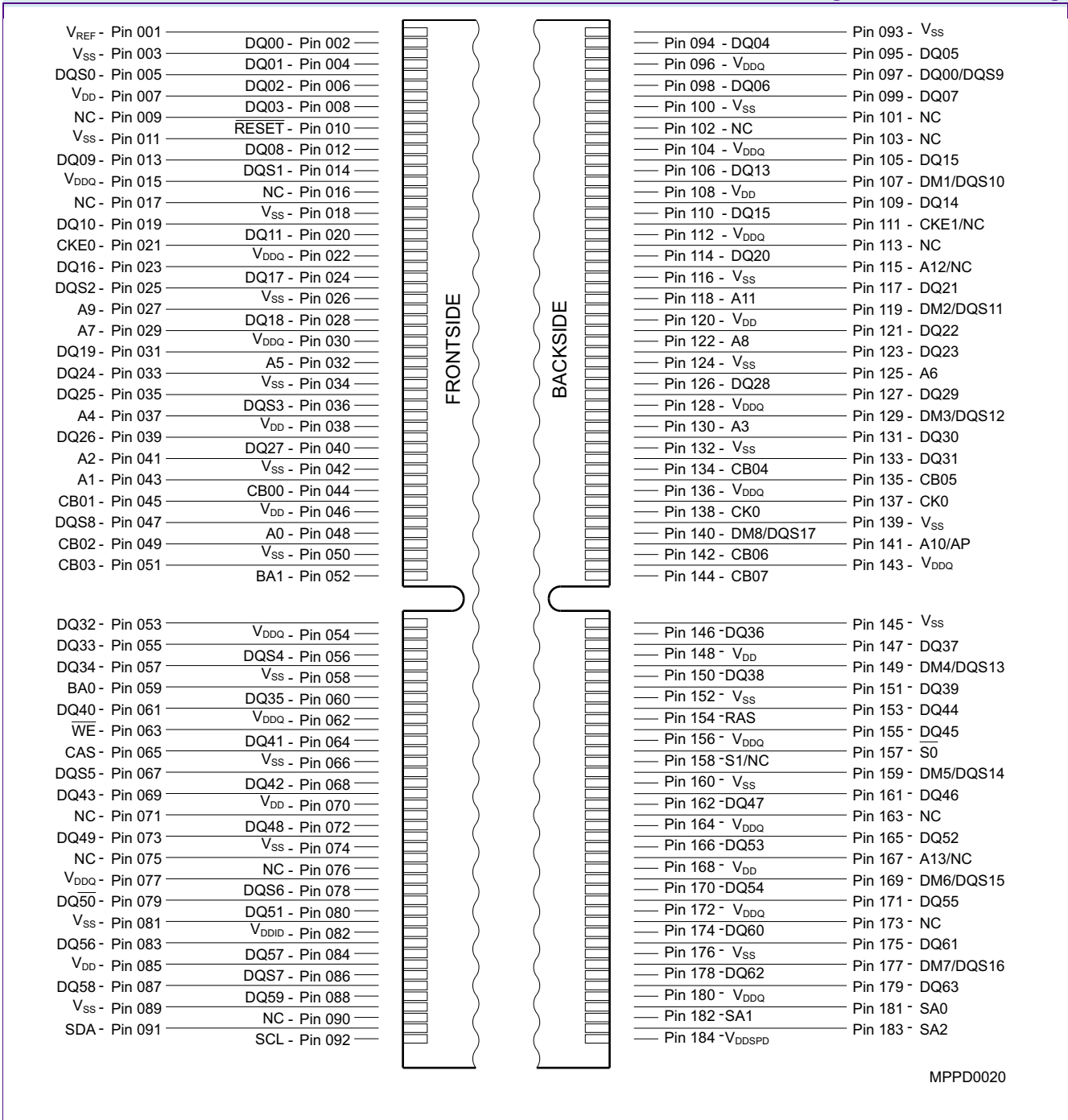
TABLE 7
Address Format

| Density | Organization | Memory Ranks | SDRAMs | # of SDRAMs | # of row/bank/ column bits | Refresh | Period | Interval |
|---------|--------------|--------------|----------|-------------|----------------------------|---------|--------|----------|
| 512 MB | 64M × 72 | 1 | 64M × 8 | 8 | 13/2/11 | 8K | 64 ms | 7.8 μs |
| 1 GB | 128M × 72 | 1 | 128M × 4 | 18 | 13/2/12 | 8K | 64 ms | 7.8 μs |
| 1 GB | 128M × 72 | 2 | 64M × 8 | 18 | 13/2/11 | 8K | 64 ms | 7.8 μs |
| 2 GB | 256M × 72 | 2 | 128M × 4 | 36 | 13/2/12 | 8K | 64 ms | 7.8 μs |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

FIGURE 1
Pin Configuration 184 Pins, Reg



MPPD0020



3 Electrical Characteristics

3.1 Operating Conditions

TABLE 8
Absolute Maximum Ratings

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--|-------------------|--------|------|-----------------|------|----------------------|
| | | Min. | Typ. | Max. | | |
| Voltage on I/O pins relative to V_{SS} | V_{IN}, V_{OUT} | -0.5 | — | $V_{DDQ} + 0.5$ | V | — |
| Voltage on inputs relative to V_{SS} | V_{IN} | -1 | — | +3.6 | V | — |
| Voltage on V_{DD} supply relative to V_{SS} | V_{DD} | -1 | — | +3.6 | V | — |
| Voltage on V_{DDQ} supply relative to V_{SS} | V_{DDQ} | -1 | — | +3.6 | V | — |
| Operating temperature (ambient) | T_A | 0 | — | +70 | °C | — |
| Storage temperature (plastic) | T_{STG} | -55 | — | +150 | °C | — |
| Power dissipation (per SDRAM component) | P_D | — | 1 | — | W | — |
| Short circuit output current | I_{OUT} | — | 50 | — | mA | — |

Attention: Permanent damage to the device may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.



TABLE 9
Electrical Characteristics and DC Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note/Test Condition ¹⁾ |
|---|-------------------|-----------------------|----------------------|-----------------------|---------|---|
| | | Min. | Typ. | Max. | | |
| Device Supply Voltage | V_{DD} | 2.3 | 2.5 | 2.7 | V | $f_{CK} \leq 166$ MHz |
| Device Supply Voltage | V_{DD} | 2.5 | 2.6 | 2.7 | V | $f_{CK} > 166$ MHz ²⁾ |
| Output Supply Voltage | V_{DDQ} | 2.3 | 2.5 | 2.7 | V | $f_{CK} \leq 166$ MHz ³⁾ |
| Output Supply Voltage | V_{DDQ} | 2.5 | 2.6 | 2.7 | V | $f_{CK} > 166$ MHz ²⁾³⁾ |
| Supply Voltage, I/O Supply Voltage | V_{SS}, V_{SSQ} | 0 | — | 0 | V | — |
| Input Reference Voltage | V_{REF} | $0.49 \times V_{DDQ}$ | $0.5 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V | 4) |
| I/O Termination Voltage (System) | V_{TT} | $V_{REF} - 0.04$ | — | $V_{REF} + 0.04$ | V | 5) |
| Input High (Logic1) Voltage | $V_{IH(DC)}$ | $V_{REF} + 0.15$ | — | $V_{DDQ} + 0.3$ | V | 6) |
| Input Low (Logic0) Voltage | $V_{IL(DC)}$ | -0.3 | — | $V_{REF} - 0.15$ | V | 6) |
| Input Voltage Level, CK and CK Inputs | $V_{IN(DC)}$ | -0.3 | — | $V_{DDQ} + 0.3$ | V | 6) |
| Input Differential Voltage, CK and \overline{CK} Inputs | $V_{ID(DC)}$ | 0.36 | — | $V_{DDQ} + 0.6$ | V | 6)7) |
| VI-Matching Pull-up Current to Pull-down Current | I_{Ratio} | 0.71 | — | 1.4 | — | 8) |
| Input Leakage Current | I_I | -2 | — | 2 | μ A | Any input $0\text{ V} \leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V ⁹⁾ |
| Output Leakage Current | I_{OZ} | -5 | — | 5 | μ A | DQs are disabled; $0\text{ V} \leq V_{OUT} \leq V_{DDQ}$ ⁹⁾ |
| Output High Current, Normal Strength Driver | I_{OH} | — | — | -16.2 | mA | $V_{OUT} = 1.95\text{ V}$ |
| Output Low Current, Normal Strength Driver | I_{OL} | 16.2 | — | — | mA | $V_{OUT} = 0.35\text{ V}$ |

- 1) $0\text{ }^\circ\text{C} \leq T_A \leq 70\text{ }^\circ\text{C}$; $V_{DDQ} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{DD} = +2.5\text{ V} \pm 0.2\text{ V}$;
- 2) DDR400 conditions apply for all clock frequencies above 166 MHz
- 3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD} .
- 4) Peak to peak AC noise on V_{REF} may not exceed $\pm 2\%$ $V_{REF,DC}$. V_{REF} is also expected to track noise variations in V_{DDQ} .
- 5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .
- 6) Inputs are not recognized as valid until V_{REF} stabilizes.
- 7) V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .
- 8) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- 9) Values are shown per pin.



TABLE 10
 I_{DD} Conditions

| Parameter | Symbol |
|--|------------|
| Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles. | I_{DD0} |
| Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet. | I_{DD1} |
| Precharge Power-Down Standby Current all banks idle; power-down mode; $CKE \leq V_{IL,MAX}$ | I_{DD2P} |
| Precharge Floating Standby Current $\overline{CS} \geq V_{IH,MIN}$, all banks idle; $CKE \geq V_{IH,MIN}$; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM. | I_{DD2F} |
| Precharge Quiet Standby Current $\overline{CS} \geq V_{IH,MIN}$, all banks idle; $CKE \geq V_{IH,MIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM; address and other control inputs stable at $\geq V_{IH,MIN}$ or $\leq V_{IL,MAX}$. | I_{DD2Q} |
| Active Power-Down Standby Current one bank active; power-down mode; $CKE \leq V_{IL,MAX}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM. | I_{DD3P} |
| Active Standby Current one bank active; $\overline{CS} \geq V_{IH,MIN}$; $CKE \geq V_{IH,MIN}$; $t_{RC} = t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle. | I_{DD3N} |
| Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50 % of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; $I_{OUT} = 0$ mA | I_{DD4R} |
| Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50 % of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B | I_{DD4W} |
| Auto-Refresh Current $t_{RC} = t_{RFCMIN}$, burst refresh | I_{DD5} |
| Self-Refresh Current $CKE \leq 0.2$ V; external clock on | I_{DD6} |
| Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet. | I_{DD7} |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

TABLE 11

I_{DD} Specification for HYS72D[64/128/256]xxx[G/H]BR-5-B

| Product Type | HYS72D64301GBR-5-B HYS72D64301HBR-5-B | | HYS72D128300GBR-5-B HYS72D128300HBR-5-B | | HYS72D128321GBR-5-B HYS72D128321HBR-5-B | | HYS72D256220GBR-5-B HYS72D256220HBR-5-B HYS72D256320HBR-5-B | | Unit | Note/ Test Conditions ^{1) 2)} |
|--------------|--|------|--|------|--|------|---|------|------|--|
| | 512 MB | | 1 GB | | 1 GB | | 2 GB | | | |
| Organization | ×72 | | ×72 | | ×72 | | ×72 | | | |
| | 1 Rank | | 1 Rank | | 2 Ranks | | 2 Ranks | | | |
| | -5 | | -5 | | -5 | | -5 | | | |
| | Symbol | Typ. | Max. | Typ. | Max. | Typ. | Max. | Typ. | Max. | |
| I_{DD0} | 1230 | 1460 | 2250 | 2660 | 1880 | 2180 | 3550 | 4110 | mA | ³⁾ |
| I_{DD1} | 1450 | 1690 | 2560 | 2980 | 2100 | 2410 | 3860 | 4430 | mA | ³⁾⁴⁾ |
| I_{DD2P} | 410 | 430 | 690 | 770 | 690 | 770 | 1320 | 1440 | mA | ⁵⁾ |
| I_{DD2F} | 880 | 990 | 1450 | 1620 | 1450 | 1620 | 2590 | 2870 | mA | ⁵⁾ |
| I_{DD2Q} | 530 | 630 | 1000 | 1160 | 1000 | 1160 | 1940 | 2230 | mA | ⁵⁾ |
| I_{DD3P} | 460 | 540 | 870 | 980 | 870 | 980 | 1690 | 1870 | mA | ⁵⁾ |
| I_{DD3N} | 960 | 1090 | 1610 | 1820 | 1610 | 1820 | 2910 | 3260 | mA | ⁵⁾ |
| I_{DD4R} | 1400 | 1600 | 2470 | 2800 | 2050 | 2320 | 3770 | 4250 | mA | ³⁾⁴⁾ |
| I_{DD4W} | 1450 | 1650 | 2560 | 2890 | 2100 | 2370 | 3860 | 4340 | mA | ³⁾ |
| I_{DD5} | 2210 | 2620 | 4360 | 5120 | 2870 | 3340 | 5660 | 6570 | mA | ³⁾ |
| I_{DD6} | 360 | 390 | 660 | 740 | 660 | 740 | 1310 | 1430 | mA | ⁵⁾ |
| I_{DD7} | 2700 | 3190 | 5620 | 6580 | 3630 | 4210 | 6920 | 8030 | mA | ³⁾⁴⁾ |

- 1) Test condition for maximum values: $V_{DD} = 2.7\text{ V}$, $T_A = 10\text{ °C}$
- 2) Module I_{DD} is calculated on the basis of component I_{DD} and includes Register and PLL currents
- 3) The module I_{DD} values are calculated from the component I_{DD} data sheet values are:
 $n * I_{DDx}[\text{component}]$ for single bank modules (n: number of components per module bank)
 $n * I_{DDx}[\text{component}] + n * I_{DD3N}[\text{component}]$ for two bank modules (n: number of components per module bank)
- 4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
- 5) The module I_{DD} values are calculated from the component I_{DD} decathlete values are:
 $n * I_{DDx}[\text{component}]$ for single bank modules (n: number of components per module bank)
 $2 * n * I_{DDx}[\text{component}]$ for single two bank modules (n: number of components per module bank)



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

TABLE 12

I_{DD} Specification for HYS72D[64/128/256]xxx[G/H]BR-6-B

| Product Type | HYS72D64301GBR-6-B HYS72D64301HBR-6-B | | HYS72D128300GBR-6-B HYS72D128300HBR-6-B | | HYS72D128321GBR-6-B HYS72D128321HBR-6-B | | HYS72D256220GBR-6-B HYS72D256320GBR-6-B HYS72D256220HBR-6-B HYS72D256320HBR-6-B | | Unit | Note/ Test Conditions ^{1) 2)} |
|--------------|--|------|--|------|--|------|--|------|------|--|
| | 512 MB | | 1 GB | | 1 GB | | 2 GB | | | |
| Organization | ×72 | | ×72 | | ×72 | | ×72 | | | |
| | 1 Rank | | 1 Rank | | 2 Ranks | | 2 Ranks | | | |
| | -6 | | -6 | | -6 | | -6 | | | |
| | | | | | | | | | | |
| Symbol | Typ. | Max. | Typ. | Max. | Typ. | Max. | Typ. | Max. | | |
| I_{DD0} | 1130 | 1320 | 2060 | 2380 | 1700 | 1940 | 3190 | 3620 | mA | ³⁾ |
| I_{DD1} | 1340 | 1540 | 2360 | 2690 | 1910 | 2160 | 3490 | 3930 | mA | ³⁾⁴⁾ |
| I_{DD2P} | 380 | 400 | 610 | 690 | 610 | 690 | 1140 | 1260 | mA | ⁵⁾ |
| I_{DD2F} | 780 | 880 | 1250 | 1400 | 1250 | 1400 | 2200 | 2440 | mA | ⁵⁾ |
| I_{DD2Q} | 480 | 580 | 890 | 1050 | 890 | 1050 | 1690 | 1980 | mA | ⁵⁾ |
| I_{DD3P} | 430 | 500 | 780 | 890 | 780 | 890 | 1480 | 1660 | mA | ⁵⁾ |
| I_{DD3N} | 870 | 980 | 1430 | 1600 | 1430 | 1600 | 2560 | 2840 | mA | ⁵⁾ |
| I_{DD4R} | 1270 | 1450 | 2210 | 2510 | 1840 | 2070 | 3340 | 3750 | mA | ³⁾⁴⁾ |
| I_{DD4W} | 1310 | 1500 | 2290 | 2600 | 1870 | 2110 | 3420 | 3840 | mA | ³⁾ |
| I_{DD5} | 2010 | 2360 | 3920 | 4590 | 2570 | 2970 | 5050 | 5820 | mA | ³⁾ |
| I_{DD6} | 350 | 390 | 600 | 680 | 600 | 680 | 1150 | 1270 | mA | ⁵⁾ |
| I_{DD7} | 2440 | 2880 | 5040 | 5910 | 3250 | 3770 | 6170 | 7150 | mA | ³⁾⁴⁾ |

- 1) Test condition for maximum values: $V_{DD} = 2.7\text{ V}$, $T_A = 10\text{ °C}$
- 2) Module I_{DD} is calculated on the basis of component I_{DD} and includes Register and PLL currents
- 3) The module I_{DD} values are calculated from the component I_{DD} decathlete values are:
 $n * I_{DD} \times [\text{component}]$ for single bank modules (n: number of components per module bank)
 $n * I_{DD} \times [\text{component}] + n * I_{DD3N} [\text{component}]$ for two bank modules (n: number of components per module bank)
- 4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
- 5) The module I_{DD} values are calculated from the component I_{DD} decathlete values are:
 $n * I_{DD} \times [\text{component}]$ for single bank modules (n: number of components per module bank)
 $2 * n * I_{DD} \times [\text{component}]$ for single two bank modules (n: number of components per module bank)



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
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TABLE 13

I_{DD} Specification for HYS72D[128/256]xxx[G/H]BR-7-B

| Product Type | HYS72D128300GBR-7-B HYS72D128300HBR-7-B | | HYS72D128321GBR-7-B HYS72D128321HBR-7-B | | HYS72D256220GBR-7-B HYS72D256320GBR-7-B HYS72D256220HBR-7-B HYS72D256320HBR-7-B | | Unit | Note/ Test Conditions ^{1) 2)} |
|--------------|--|------|--|------|--|------|------|--|
| | 1 GB | | 1 GB | | 2 GB | | | |
| Organization | ×72 | | ×72 | | ×72 | | | |
| | 1 Rank | | 2 Ranks | | 2 Ranks | | | |
| | -7 | | -7 | | -7 | | | |
| | | | | | | | | |
| Symbol | Typ. | Max. | Typ. | Max. | Typ. | Max. | | |
| I_{DD0} | 1780 | 2060 | 1460 | 1670 | 2700 | 3090 | mA | 3) |
| I_{DD1} | 2070 | 2390 | 1650 | 1900 | 2990 | 3420 | mA | 3)4) |
| I_{DD2P} | 530 | 610 | 530 | 610 | 960 | 1080 | mA | 5) |
| I_{DD2F} | 1050 | 1180 | 1050 | 1180 | 1810 | 2010 | mA | 5) |
| I_{DD2Q} | 770 | 910 | 770 | 910 | 1440 | 1690 | mA | 5) |
| I_{DD3P} | 660 | 770 | 660 | 770 | 1230 | 1400 | mA | 5) |
| I_{DD3N} | 1210 | 1380 | 1210 | 1380 | 2140 | 2410 | mA | 5) |
| I_{DD4R} | 1920 | 2170 | 1580 | 1790 | 2840 | 3200 | mA | 3)4) |
| I_{DD4W} | 1990 | 2260 | 1620 | 1830 | 2920 | 3290 | mA | 3) |
| I_{DD5} | 3570 | 4230 | 2300 | 2700 | 4490 | 5260 | mA | 3) |
| I_{DD6} | 540 | 620 | 540 | 620 | 990 | 1110 | mA | 5) |
| I_{DD7} | 4390 | 5140 | 2810 | 3270 | 5310 | 6170 | mA | 3)4) |

- 1) Test condition for maximum values: $V_{DD} = 2.7\text{ V}$, $T_A = 10\text{ °C}$
- 2) Module I_{DD} is calculated on the basis of component I_{DD} and includes Register an PLL
- 3) The module I_{DD} values are calculated from the component I_{DD} decathlete values are:
 $n * I_{DD} \times [\text{component}]$ for single bank modules (n: number of components per module bank)
 $n * I_{DD} \times [\text{component}] + n * I_{DD3N} [\text{component}]$ for two bank modules (n: number of components per module bank)
- 4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
- 5) The module I_{DD} values are calculated from the component I_{DD} decathlete values are:
 $n * I_{DD} \times [\text{component}]$ for single bank modules (n: number of components per module bank)
 $2 * n * I_{DD} \times [\text{component}]$ for single two bank modules (n: number of components per module bank)



TABLE 14
AC Timing - Absolute Specifications for PC3200 and PC2700

| Parameter | Symbol | -5 | | -6 | | Unit | Note/ Test Condition ¹⁾ |
|--|--------------|-----------------------------------|-------|------------------------------|-------|----------|------------------------------------|
| | | DDR400B | | DDR333 | | | |
| | | Min. | Max. | Min. | Max. | | |
| DQ output access time from CK/CK | t_{AC} | -0.5 | +0.5 | -0.7 | +0.7 | ns | 2)3)4)5) |
| CK high-level width | t_{CH} | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | 2)3)4)5) |
| Clock cycle time | t_{CK} | 5 | 8 | 6 | 12 | ns | CL = 3.0 2)3)4)5) |
| | | 6 | 12 | 6 | 12 | ns | CL = 2.5 2)3)4)5) |
| | | 7.5 | 12 | 7.5 | 12 | ns | CL = 2.0 2)3)4)5) |
| CK low-level width | t_{CL} | 0.45 | 0.55 | 0.45 | 0.55 | t_{CK} | 2)3)4)5) |
| Auto precharge write recovery + precharge time | t_{DAL} | $(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$ | | | | t_{CK} | 2)3)4)5)6) |
| DQ and DM input hold time | t_{DH} | 0.4 | — | 0.45 | — | ns | 2)3)4)5) |
| DQ and DM input pulse width (each input) | t_{DIPW} | 1.75 | — | 1.75 | — | ns | 2)3)4)5)6) |
| DQS output access time from CK/CK | t_{DQSK} | -0.6 | +0.6 | -0.6 | +0.6 | ns | 2)3)4)5) |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | 0.35 | — | t_{CK} | 2)3)4)5) |
| DQS-DQ skew (DQS and associated DQ signals) | t_{DQSQ} | — | +0.40 | — | +0.40 | ns | TFBGA 2)3)4)5) |
| Write command to 1 st DQS latching transition | t_{DQSS} | 0.72 | 1.25 | 0.75 | 1.25 | t_{CK} | 2)3)4)5) |
| DQ and DM input setup time | t_{DS} | 0.4 | — | 0.45 | — | ns | 2)3)4)5) |
| DQS falling edge hold time from CK (write cycle) | t_{DSH} | 0.2 | — | 0.2 | — | t_{CK} | 2)3)4)5) |
| DQS falling edge to CK setup time (write cycle) | t_{DSS} | 0.2 | — | 0.2 | — | t_{CK} | 2)3)4)5) |
| Clock Half Period | t_{HP} | Min. (t_{CL} , t_{CH}) | — | Min. (t_{CL} , t_{CH}) | — | ns | 2)3)4)5) |
| Data-out high-impedance time from CK/CK | t_{HZ} | — | +0.7 | — | +0.7 | ns | 2)3)4)5)7) |
| Address and control input hold time | t_{IH} | 0.6 | — | 0.75 | — | ns | Fast slew rate 3)4)5)6)8) |
| | | 0.7 | — | 0.8 | — | ns | Slow slew rate 3)4)5)6)8) |
| Control and Addr. input pulse width (each input) | t_{IPW} | 2.2 | — | 2.2 | — | ns | 2)3)4)5)9) |
| Address and control input setup time | t_{IS} | 0.6 | — | 0.75 | — | ns | Fast slew rate 3)4)5)6)8) |
| | | 0.7 | — | 0.8 | — | ns | Slow slew rate 3)4)5)6)8) |



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| Parameter | Symbol | -5 | | -6 | | Unit | Note/ Test Condition ¹⁾ |
|---|--------------------|----------------------------------|-------|----------------------------------|-------|-----------------|------------------------------------|
| | | DDR400B | | DDR333 | | | |
| | | Min. | Max. | Min. | Max. | | |
| Data-out low-impedance time from CK/ $\overline{\text{CK}}$ | t_{LZ} | -0.7 | +0.7 | -0.7 | +0.7 | ns | 2)3)4)5)7) |
| Mode register set command cycle time | t_{MRD} | 2 | — | 2 | — | t_{CK} | 2)3)4)5) |
| DQ/DQS output hold time from DQS | t_{QH} | $t_{\text{HP}} - t_{\text{QHS}}$ | — | $t_{\text{HP}} - t_{\text{QHS}}$ | — | ns | 2)3)4)5) |
| Data hold skew factor | t_{QHS} | — | +0.50 | — | +0.50 | ns | TFBGA 2)3)4)5) |
| Active to Autoprecharge delay | t_{RAP} | t_{RCD} | — | t_{RCD} | — | ns | 2)3)4)5) |
| Active to Precharge command | t_{RAS} | 40 | 70E+3 | 42 | 70E+3 | ns | 2)3)4)5) |
| Active to Active/Auto-refresh command period | t_{RC} | 55 | — | 60 | — | ns | 2)3)4)5) |
| Active to Read or Write delay | t_{RCD} | 15 | — | 18 | — | ns | 2)3)4)5) |
| Average Periodic Refresh Interval | t_{REFI} | — | 7.8 | — | 7.8 | μs | 2)3)4)5)10) |
| Auto-refresh to Active/Auto-refresh command period | t_{RFC} | 65 | — | 72 | — | ns | 2)3)4)5) |
| Precharge command period | t_{RP} | 15 | — | 18 | — | ns | 2)3)4)5) |
| Read preamble | t_{RPRE} | 0.9 | 1.1 | 0.9 | 1.1 | t_{CK} | 2)3)4)5) |
| Read postamble | t_{RPST} | 0.40 | 0.60 | 0.40 | 0.60 | t_{CK} | 2)3)4)5) |
| Active bank A to Active bank B command | t_{RRD} | 10 | — | 12 | — | ns | 2)3)4)5) |
| Write preamble | t_{WPRE} | 0.25 | — | 0.25 | — | t_{CK} | 2)3)4)5) |
| Write preamble setup time | t_{WPRES} | 0 | — | 0 | — | ns | 2)3)4)5)11) |
| Write postamble | t_{WPST} | 0.40 | 0.60 | 0.40 | 0.60 | t_{CK} | 2)3)4)5)12) |
| Write recovery time | t_{WR} | 15 | — | 15 | — | ns | 2)3)4)5) |
| Internal write to read command delay | t_{WTR} | 2 | — | 1 | — | t_{CK} | 2)3)4)5) |
| Exit self-refresh to non-read command | t_{XSNR} | 75 | — | 75 | — | ns | 2)3)4)5) |
| Exit self-refresh to read command | t_{XSRD} | 200 | — | 200 | — | t_{CK} | 2)3)4)5) |

- 1) $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$; $V_{\text{DDQ}} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{\text{DD}} = +2.5\text{ V} \pm 0.2\text{ V}$ (DDR333); $V_{\text{DDQ}} = 2.6\text{ V} \pm 0.1\text{ V}$, $V_{\text{DD}} = +2.6\text{ V} \pm 0.1\text{ V}$ (DDR400)
- 2) Input slew rate $\geq 1\text{ V/ns}$ for DDR400, DDR333
- 3) The CK/ $\overline{\text{CK}}$ input reference level (for timing reference to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross: the input reference level for signals other than CK/ $\overline{\text{CK}}$, is V_{REF} . CK/ $\overline{\text{CK}}$ slew rate are $\geq 1.0\text{ V/ns}$.
- 4) Inputs are not recognized as valid until V_{REF} stabilizes.
- 5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT} .
- 6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.
- 7) t_{HZHZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- 8) Fast slew rate $\geq 1.0\text{ V/ns}$, slow slew rate $\geq 0.5\text{ V/ns}$ and $< 1\text{ V/ns}$ for command/address and CK & $\overline{\text{CK}}$ slew rate $> 1.0\text{ V/ns}$, measured between $V_{\text{IH(ac)}}$ and $V_{\text{IL(ac)}}$.
- 9) These parameters guarantee device timing, but they are not necessarily tested on each device.
- 10) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.



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- 11) The specific requirement is that DQS be valid (HIGH,LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW at this time, depending on t_{DQSS} .
- 12) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

TABLE 15

AC Timing - Absolute Specifications for PC2100

| Parameter | Symbol | -7 | | Unit | Note/Test Condition ¹⁾ |
|--|--------------|-----------------------------------|-------|----------|-----------------------------------|
| | | DDR266A | | | |
| | | Min. | Max. | | |
| DQ output access time from CK/CK | t_{AC} | -0.75 | +0.75 | ns | 2)3)4)5) |
| CK high-level width | t_{CH} | 0.45 | 0.55 | t_{CK} | 2)3)4)5) |
| Clock cycle time | t_{CK} | 7 | 12 | — | CL = 3 ²⁾³⁾⁴⁾⁵⁾ |
| | | 7.5 | 12 | ns | CL = 2.5 ²⁾³⁾⁴⁾⁵⁾ |
| | | 7.5 | 12 | ns | CL = 2.0 ²⁾³⁾⁴⁾⁵⁾ |
| CK low-level width | t_{CL} | 0.45 | 0.55 | t_{CK} | 2)3)4)5) |
| Auto precharge write recovery + precharge time | t_{DAL} | $(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$ | — | t_{CK} | 2)3)4)5)6) |
| DQ and DM input hold time | t_{DH} | 0.5 | — | ns | 2)3)4)5) |
| DQ and DM input pulse width (each input) | t_{DIPW} | 1.75 | — | ns | 2)3)4)5)6) |
| DQS output access time from CK/CK | t_{DQSCK} | -0.75 | +0.75 | ns | 2)3)4)5) |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | t_{CK} | 2)3)4)5) |
| DQS-DQ skew (DQS and associated DQ signals) | t_{DQSQ} | — | +0.5 | ns | FBGA ²⁾³⁾⁴⁾⁵⁾ |
| Write command to 1 st DQS latching transition | t_{DQSS} | 0.75 | 1.25 | t_{CK} | 2)3)4)5) |
| DQ and DM input setup time | t_{DS} | 0.5 | — | ns | 2)3)4)5) |
| DQS falling edge hold time from CK (write cycle) | t_{DSH} | 0.2 | — | t_{CK} | 2)3)4)5) |
| DQS falling edge to CK setup time (write cycle) | t_{DSS} | 0.2 | — | t_{CK} | 2)3)4)5) |
| Clock Half Period | t_{HP} | min. (t_{CL} , t_{CH}) | — | ns | 2)3)4)5) |
| Data-out high-impedance time from CK/CK | t_{HZ} | — | +0.75 | ns | 2)3)4)5)7) |
| Address and control input hold time | t_{IH} | 0.9 | — | ns | fast slew rate 3)4)5)6)8) |
| | | 1.0 | — | ns | slow slew rate 3)4)5)6)8) |
| Control and Addr. input pulse width (each input) | t_{IPW} | 2.2 | — | ns | 2)3)4)5)9) |
| Address and control input setup time | t_{IS} | 0.9 | — | ns | fast slew rate 3)4)5)6)8) |
| | | 1.0 | — | ns | slow slew rate 3)4)5)6)8) |
| Data-out low-impedance time from CK/CK | t_{LZ} | -0.75 | +0.75 | ns | 2)3)4)5)7) |
| Mode register set command cycle time | t_{MRD} | 2 | — | t_{CK} | 2)3)4)5) |
| DQ/DQS output hold time from DQS | t_{QH} | $t_{HP} - t_{QHS}$ | — | ns | 2)3)4)5) |
| Data hold skew factor | t_{QHS} | — | 0.75 | ns | FBGA ²⁾³⁾⁴⁾⁵⁾ |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Parameter | Symbol | -7 | | Unit | Note/Test Condition ¹⁾ |
|--|-------------|-----------|--------|----------|-----------------------------------|
| | | DDR266A | | | |
| | | Min. | Max. | | |
| Active to Read w/AP delay | t_{RAP} | t_{RCD} | — | ns | 2)3)4)5) |
| Active to Precharge command | t_{RAS} | 45 | 120E+3 | ns | 2)3)4)5) |
| Active to Active/Auto-refresh command period | t_{RC} | 65 | — | ns | 2)3)4)5) |
| Active to Read or Write delay | t_{RCD} | 20 | — | ns | 2)3)4)5) |
| Average Periodic Refresh Interval | t_{REFI} | 7.8 | — | μ s | 2)3)4)5)10) |
| Auto-refresh to Active/Auto-refresh command period | t_{RFC} | 75 | — | ns | 2)3)4)5) |
| Precharge command period | t_{RP} | 20 | — | ns | 2)3)4)5) |
| Read preamble | t_{RPRE} | 0.9 | 1.1 | t_{CK} | 2)3)4)5) |
| Read postamble | t_{RPST} | 0.4 | 0.6 | t_{CK} | 2)3)4)5) |
| Active bank A to Active bank B command | t_{RRD} | 15 | — | ns | 2)3)4)5) |
| Write preamble | t_{WPRE} | 0.25 | — | t_{CK} | 2)3)4)5) |
| Write preamble setup time | t_{WPRES} | 0 | — | ns | 2)3)4)5)11) |
| Write postamble | t_{WPST} | 0.4 | — | t_{CK} | 2)3)4)5)12) |
| Write recovery time | t_{WR} | 15 | — | ns | 2)3)4)5) |
| Internal write to read command delay | t_{WTR} | 1 | — | t_{CK} | 2)3)4)5) |
| Exit self-refresh to non-read command | t_{XSNR} | 75 | — | ns | 2)3)4)5)13) |
| Exit self-refresh to read command | t_{XSRD} | 200 | — | t_{CK} | 2)3)4)5) |

- 1) $V_{DDQ} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{DD} = +2.5\text{ V} \pm 0.2\text{ V}$; $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$
- 2) Input slew rate $\geq 1\text{ V/ns}$
- 3) The CK/ $\overline{\text{CK}}$ input reference level (for timing reference to CK/ $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross: the input reference level for signals other than CK/ $\overline{\text{CK}}$, is V_{REF} . CK/ $\overline{\text{CK}}$ slew rate are $\geq 1.0\text{ V/ns}$.
- 4) Inputs are not recognized as valid until V_{REF} stabilizes.
- 5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT} .
- 6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.
- 7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- 8) Fast slew rate $\geq 1.0\text{ V/ns}$, slow slew rate $\geq 0.5\text{ V/ns}$ and $< 1\text{ V/ns}$ for command/address and CK & $\overline{\text{CK}}$ slew rate $> 1.0\text{ V/ns}$, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.
- 9) These parameters guarantee device timing, but they are not necessarily tested on each device.
- 10) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
- 11) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS} .
- 12) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 13) In all circumstances, t_{XSNR} can be satisfied using $t_{XSNR} = t_{RFC,min} + 1 \times t_{CK}$



4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- Table 16 “HYS72D[64/128/256]xxxGBR-5-B” on Page 23
- Table 17 “HYS72D[64/128/256]xxxGBR-6-B” on Page 27
- Table 18 “HYS72D[128/256]xxxGBR-7-B” on Page 31
- Table 19 “HYS72D[128/256]xxxHBR-5-B” on Page 35
- Table 20 “HYS72D[128/256]xxxHBR-6-B” on Page 39
- Table 21 “HYS72D[128/256]xxxHBR-7-B” on Page 43

TABLE 16

HYS72D[64/128/256]xxxGBR-5-B

| Product Type | | HYS72D64301GBR-5-B | HYS72D128300GBR-5-B | HYS72D128321GBR-5-B | HYS72D256220GBR-5-B |
|--------------------|--|--------------------|---------------------|---------------------|---------------------|
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 0 | Programmed SPD Bytes in E ² PROM | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in E ² PROM | 08 | 08 | 08 | 08 |
| 2 | Memory Type (DDR = 07h) | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 0B | 0C | 0B | 0C |
| 5 | Number of DIMM Ranks | 01 | 01 | 02 | 02 |
| 6 | Data Width (LSB) | 48 | 48 | 48 | 48 |
| 7 | Data Width (MSB) | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 | 04 | 04 |
| 9 | t _{CK} @ CL _{max} (Byte 18) [ns] | 50 | 50 | 50 | 50 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Product Type | | HYS72D64301GBR-5-B | HYS72D128300GBR-5-B | HYS72D128321GBR-5-B | HYS72D256220GBR-5-B |
|--------------------|--|--------------------|---------------------|---------------------|---------------------|
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 10 | t _{AC} SDRAM @ CL _{max} (Byte 18) [ns] | 50 | 50 | 50 | 50 |
| 11 | Error Correction Support | 02 | 02 | 02 | 02 |
| 12 | Refresh Rate | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM Width | 08 | 04 | 08 | 04 |
| 14 | Error Checking SDRAM Width | 08 | 04 | 08 | 04 |
| 15 | t _{CCD} [cycles] | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E | 0E | 0E |
| 17 | Number of Banks on SDRAM Device | 04 | 04 | 04 | 04 |
| 18 | CAS Latency | 1C | 1C | 1C | 1C |
| 19 | CS Latency | 01 | 01 | 01 | 01 |
| 20 | Write Latency | 02 | 02 | 02 | 02 |
| 21 | DIMM Attributes | 26 | 26 | 26 | 26 |
| 22 | Component Attributes | C1 | C1 | C1 | C1 |
| 23 | t _{CK} @ CL _{max} -0.5 (Byte 18) [ns] | 60 | 60 | 60 | 60 |
| 24 | t _{AC} SDRAM @ CL _{max} -0.5 [ns] | 50 | 50 | 50 | 50 |
| 25 | t _{CK} @ CL _{max} -1 (Byte 18) [ns] | 75 | 75 | 75 | 75 |
| 26 | t _{AC} SDRAM @ CL _{max} -1 [ns] | 50 | 50 | 50 | 50 |
| 27 | t _{RPmin} [ns] | 3C | 3C | 3C | 3C |
| 28 | t _{RRDmin} [ns] | 28 | 28 | 28 | 28 |
| 29 | t _{RCDmin} [ns] | 3C | 3C | 3C | 3C |
| 30 | t _{RASmin} [ns] | 28 | 28 | 28 | 28 |
| 31 | Module Density per Rank | 80 | 01 | 80 | 01 |
| 32 | t _{AS} , t _{CS} [ns] | 60 | 60 | 60 | 60 |
| 33 | t _{AH} , t _{CH} [ns] | 60 | 60 | 60 | 60 |
| 34 | t _{DS} [ns] | 40 | 40 | 40 | 40 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Product Type | | HYS72D64301GBR-5-B | HYS72D128300GBR-5-B | HYS72D128321GBR-5-B | HYS72D256220GBR-5-B |
|--------------------|----------------------------------|--------------------|---------------------|---------------------|---------------------|
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 35 | t _{DH} [ns] | 40 | 40 | 40 | 40 |
| 36 - 40 | Not used | 00 | 00 | 00 | 00 |
| 41 | t _{RCmin} [ns] | 37 | 37 | 37 | 37 |
| 42 | t _{RFCmin} [ns] | 41 | 41 | 41 | 41 |
| 43 | t _{CKmax} [ns] | 28 | 28 | 28 | 28 |
| 44 | t _{DQSQmax} [ns] | 28 | 28 | 28 | 28 |
| 45 | t _{QHSmax} [ns] | 50 | 50 | 50 | 50 |
| 46 | not used | 00 | 00 | 00 | 00 |
| 47 | DIMM PCB Height | 01 | 01 | 01 | 01 |
| 48 - 61 | Not used | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | 10 | 10 | 10 | 10 |
| 63 | Checksum of Byte 0-62 | 67 | E1 | 68 | E2 |
| 64 | Manufacturer's JEDEC ID Code (1) | 7F | 7F | 7F | 7F |
| 65 | Manufacturer's JEDEC ID Code (2) | 7F | 7F | 7F | 7F |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx | xx | xx |
| 73 | Part Number, Char 1 | 37 | 37 | 37 | 37 |
| 74 | Part Number, Char 2 | 32 | 32 | 32 | 32 |
| 75 | Part Number, Char 3 | 44 | 44 | 44 | 44 |
| 76 | Part Number, Char 4 | 36 | 31 | 31 | 32 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | |
|---------------------------|--------------------------------|---------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D64301GBR-5-B | HYS72D128300GBR-5-B | HYS72D128321GBR-5-B | HYS72D256220GBR-5-B |
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) |
| Label Code | | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 77 | Part Number, Char 5 | 34 | 32 | 32 | 35 |
| 78 | Part Number, Char 6 | 33 | 38 | 38 | 36 |
| 79 | Part Number, Char 7 | 30 | 33 | 33 | 32 |
| 80 | Part Number, Char 8 | 31 | 30 | 32 | 32 |
| 81 | Part Number, Char 9 | 47 | 30 | 31 | 30 |
| 82 | Part Number, Char 10 | 42 | 47 | 47 | 47 |
| 83 | Part Number, Char 11 | 52 | 42 | 42 | 42 |
| 84 | Part Number, Char 12 | 35 | 52 | 52 | 52 |
| 85 | Part Number, Char 13 | 42 | 35 | 35 | 35 |
| 86 | Part Number, Char 14 | 20 | 42 | 42 | 42 |
| 87 | Part Number, Char 15 | 20 | 20 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 | 20 | 20 |
| 89 | Part Number, Char 17 | 20 | 20 | 20 | 20 |
| 90 | Part Number, Char 18 | 20 | 20 | 20 | 20 |
| 91 | Module Revision Code | 0x | 1x | 1x | 1x |
| 92 | Test Program Revision Code | xx | xx | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx | xx | xx |
| 99 - 127 | Not used | 00 | 00 | 00 | 00 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

TABLE 17
HYS72D[64/128/256]xxxGBR-6-B

| Product Type | | HYS72D64301GBR-6-B | HYS72D128300GBR-6-B | HYS72D128321GBR-6-B | HYS72D256320GBR-6-B | HYS72D256220GBR-6-B |
|--------------------|--|--------------------------------|----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| Organization | | 512MB ×72 1 Rank (×8) | 1 GByte ×72 1 Rank (×4) | 1 GByte ×72 2 Ranks (×8) | 2 GByte ×72 2 Ranks (×4) | 2 GByte ×72 2 Ranks (×4) |
| Label Code | | PC2700R-25331 | PC2700R-25330 | PC2700R-25330 | PC2700R-25330 | PC2700R-25331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 0.0 | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 0 | Programmed SPD Bytes in E ² PROM | 80 | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in E ² PROM | 08 | 08 | 08 | 08 | 08 |
| 2 | Memory Type (DDR = 07h) | 07 | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 0D | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 0B | 0C | 0B | 0C | 0C |
| 5 | Number of DIMM Ranks | 01 | 01 | 02 | 02 | 02 |
| 6 | Data Width (LSB) | 48 | 48 | 48 | 48 | 48 |
| 7 | Data Width (MSB) | 00 | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 | 04 | 04 | 04 |
| 9 | t _{CK} @ CL _{max} (Byte 18) [ns] | 60 | 60 | 60 | 60 | 60 |
| 10 | t _{AC} SDRAM @ CL _{max} (Byte 18) [ns] | 70 | 70 | 70 | 70 | 70 |
| 11 | Error Correction Support | 02 | 02 | 02 | 02 | 02 |
| 12 | Refresh Rate | 82 | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM Width | 08 | 04 | 08 | 04 | 04 |
| 14 | Error Checking SDRAM Width | 08 | 04 | 08 | 04 | 04 |
| 15 | t _{CCD} [cycles] | 01 | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E | 0E | 0E | 0E |
| 17 | Number of Banks on SDRAM Device | 04 | 04 | 04 | 04 | 04 |
| 18 | CAS Latency | 0C | 0C | 0C | 0C | 0C |
| 19 | CS Latency | 01 | 01 | 01 | 01 | 01 |
| 20 | Write Latency | 02 | 02 | 02 | 02 | 02 |
| 21 | DIMM Attributes | 26 | 26 | 26 | 26 | 26 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Product Type | | HYS72D64301GBR-6-B | HYS72D128300GBR-6-B | HYS72D128321GBR-6-B | HYS72D256320GBR-6-B | HYS72D256220GBR-6-B |
|--------------------|---|--------------------|---------------------|---------------------|---------------------|---------------------|
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2700R-25331 | PC2700R-25330 | PC2700R-25330 | PC2700R-25330 | PC2700R-25331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 0.0 | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 22 | Component Attributes | C1 | C1 | C1 | C1 | C1 |
| 23 | t _{CK} @ CL _{max} -0.5 (Byte 18) [ns] | 75 | 75 | 75 | 75 | 75 |
| 24 | t _{AC} SDRAM @ CL _{max} -0.5 [ns] | 70 | 70 | 70 | 70 | 70 |
| 25 | t _{CK} @ CL _{max} -1 (Byte 18) [ns] | 00 | 00 | 00 | 00 | 00 |
| 26 | t _{AC} SDRAM @ CL _{max} -1 [ns] | 00 | 00 | 00 | 00 | 00 |
| 27 | t _{RPmin} [ns] | 48 | 48 | 48 | 48 | 48 |
| 28 | t _{RRDmin} [ns] | 30 | 30 | 30 | 30 | 30 |
| 29 | t _{RCDmin} [ns] | 48 | 48 | 48 | 48 | 48 |
| 30 | t _{RASmin} [ns] | 2A | 2A | 2A | 2A | 2A |
| 31 | Module Density per Rank | 80 | 01 | 80 | 01 | 01 |
| 32 | t _{AS} , t _{CS} [ns] | 75 | 75 | 75 | 75 | 75 |
| 33 | t _{AH} , t _{CH} [ns] | 75 | 75 | 75 | 75 | 75 |
| 34 | t _{DS} [ns] | 45 | 45 | 45 | 45 | 45 |
| 35 | t _{DH} [ns] | 45 | 45 | 45 | 45 | 45 |
| 36 - 40 | Not used | 00 | 00 | 00 | 00 | 00 |
| 41 | t _{RCmin} [ns] | 3C | 3C | 3C | 3C | 3C |
| 42 | t _{RFCmin} [ns] | 48 | 48 | 48 | 48 | 48 |
| 43 | t _{CKmax} [ns] | 30 | 30 | 30 | 30 | 30 |
| 44 | t _{DQSQmax} [ns] | 28 | 28 | 28 | 28 | 28 |
| 45 | t _{QHSmax} [ns] | 50 | 50 | 50 | 50 | 50 |
| 46 | not used | 00 | 00 | 00 | 00 | 00 |
| 47 | DIMM PCB Height | 01 | 00 | 00 | 00 | 01 |
| 48 - 61 | Not used | 00 | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | 10 | 00 | 00 | 00 | 10 |
| 63 | Checksum of Byte 0-62 | 61 | CA | 51 | CB | DC |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | | |
|---------------------------|----------------------------------|---------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D64301GBR-6-B | HYS72D128300GBR-6-B | HYS72D128321GBR-6-B | HYS72D256320GBR-6-B | HYS72D256220GBR-6-B |
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2700R-25331 | PC2700R-25330 | PC2700R-25330 | PC2700R-25330 | PC2700R-25331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 0.0 | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 64 | Manufacturer's JEDEC ID Code (1) | 7F | 7F | 7F | 7F | 7F |
| 65 | Manufacturer's JEDEC ID Code (2) | 7F | 7F | 7F | 7F | 7F |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F | 7F | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F | 7F | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F | 7F | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 | 51 | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 | 00 | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 | 00 | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx | xx | xx | xx |
| 73 | Part Number, Char 1 | 37 | 37 | 37 | 37 | 37 |
| 74 | Part Number, Char 2 | 32 | 32 | 32 | 32 | 32 |
| 75 | Part Number, Char 3 | 44 | 44 | 44 | 44 | 44 |
| 76 | Part Number, Char 4 | 36 | 31 | 31 | 32 | 32 |
| 77 | Part Number, Char 5 | 34 | 32 | 32 | 35 | 35 |
| 78 | Part Number, Char 6 | 33 | 38 | 38 | 36 | 36 |
| 79 | Part Number, Char 7 | 30 | 33 | 33 | 33 | 32 |
| 80 | Part Number, Char 8 | 31 | 30 | 32 | 32 | 32 |
| 81 | Part Number, Char 9 | 47 | 30 | 31 | 30 | 30 |
| 82 | Part Number, Char 10 | 42 | 47 | 47 | 47 | 47 |
| 83 | Part Number, Char 11 | 52 | 42 | 42 | 42 | 42 |
| 84 | Part Number, Char 12 | 36 | 52 | 52 | 52 | 52 |
| 85 | Part Number, Char 13 | 42 | 36 | 36 | 36 | 36 |
| 86 | Part Number, Char 14 | 20 | 42 | 42 | 42 | 42 |
| 87 | Part Number, Char 15 | 20 | 20 | 20 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 | 20 | 20 | 20 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | | |
|---------------------------|--------------------------------|---------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D64301GBR-6-B | HYS72D128300GBR-6-B | HYS72D128321GBR-6-B | HYS72D256320GBR-6-B | HYS72D256220GBR-6-B |
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2700R-25331 | PC2700R-25330 | PC2700R-25330 | PC2700R-25330 | PC2700R-25331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 0.0 | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 89 | Part Number, Char 17 | 20 | 20 | 20 | 20 | 20 |
| 90 | Part Number, Char 18 | 20 | 20 | 20 | 20 | 20 |
| 91 | Module Revision Code | 0x | 1x | 1x | 1x | 1x |
| 92 | Test Program Revision Code | xx | xx | xx | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx | xx | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx | xx | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx | xx | xx | xx |
| 99 - 127 | Not used | 00 | 00 | 00 | 00 | 00 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

TABLE 18
HYS72D[128/256]xxxGBR-7-B

| Product Type | | HYS72D128300GBR-7-B | HYS72D128321GBR-7-B | HYS72D256220GBR-7-B | HYS72D256320GBR-7-B |
|--------------------|--|---------------------|---------------------|---------------------|---------------------|
| Organization | | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2100R-20330 | PC2100R-20330 | PC2100R-20331 | PC2100R-20330 |
| JEDEC SPD Revision | | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 0 | Programmed SPD Bytes in E ² PROM | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in E ² PROM | 08 | 08 | 08 | 08 |
| 2 | Memory Type (DDR = 07h) | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 0C | 0B | 0C | 0C |
| 5 | Number of DIMM Ranks | 01 | 02 | 02 | 02 |
| 6 | Data Width (LSB) | 48 | 48 | 48 | 48 |
| 7 | Data Width (MSB) | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 | 04 | 04 |
| 9 | t _{CK} @ CL _{max} (Byte 18) [ns] | 70 | 70 | 70 | 70 |
| 10 | t _{AC} SDRAM @ CL _{max} (Byte 18) [ns] | 75 | 75 | 75 | 75 |
| 11 | Error Correction Support | 02 | 02 | 02 | 02 |
| 12 | Refresh Rate | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM Width | 04 | 08 | 04 | 04 |
| 14 | Error Checking SDRAM Width | 04 | 08 | 04 | 04 |
| 15 | t _{CCD} [cycles] | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E | 0E | 0E |
| 17 | Number of Banks on SDRAM Device | 04 | 04 | 04 | 04 |
| 18 | CAS Latency | 0C | 0C | 0C | 0C |
| 19 | CS Latency | 01 | 01 | 01 | 01 |
| 20 | Write Latency | 02 | 02 | 02 | 02 |
| 21 | DIMM Attributes | 26 | 26 | 26 | 26 |
| 22 | Component Attributes | C1 | C1 | C1 | C1 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Product Type | | HYS72D128300GBR-7-B | HYS72D128321GBR-7-B | HYS72D256220GBR-7-B | HYS72D256320GBR-7-B |
|--------------------|---|---------------------|---------------------|---------------------|---------------------|
| Organization | | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2100R-20330 | PC2100R-20330 | PC2100R-20331 | PC2100R-20330 |
| JEDEC SPD Revision | | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 23 | t _{CK} @ CL _{max} -0.5 (Byte 18) [ns] | 75 | 75 | 75 | 75 |
| 24 | t _{AC} SDRAM @ CL _{max} -0.5 [ns] | 75 | 75 | 75 | 75 |
| 25 | t _{CK} @ CL _{max} -1 (Byte 18) [ns] | 00 | 00 | 00 | 00 |
| 26 | t _{AC} SDRAM @ CL _{max} -1 [ns] | 00 | 00 | 00 | 00 |
| 27 | t _{RPmin} [ns] | 50 | 50 | 50 | 50 |
| 28 | t _{RRDmin} [ns] | 3C | 3C | 3C | 3C |
| 29 | t _{RCDmin} [ns] | 50 | 50 | 50 | 50 |
| 30 | t _{RASmin} [ns] | 2D | 2D | 2D | 2D |
| 31 | Module Density per Rank | 01 | 80 | 01 | 01 |
| 32 | t _{AS} , t _{CS} [ns] | 90 | 90 | 90 | 90 |
| 33 | t _{AH} , t _{CH} [ns] | 90 | 90 | 90 | 90 |
| 34 | t _{DS} [ns] | 50 | 50 | 50 | 50 |
| 35 | t _{DH} [ns] | 50 | 50 | 50 | 50 |
| 36 - 40 | Not used | 00 | 00 | 00 | 00 |
| 41 | t _{RCmin} [ns] | 41 | 41 | 41 | 41 |
| 42 | t _{RFCmin} [ns] | 4B | 4B | 4B | 4B |
| 43 | t _{CKmax} [ns] | 30 | 30 | 30 | 30 |
| 44 | t _{DQSQmax} [ns] | 32 | 32 | 32 | 32 |
| 45 | t _{QHSmax} [ns] | 75 | 75 | 75 | 75 |
| 46 | not used | 00 | 00 | 00 | 00 |
| 47 | DIMM PCB Height | 00 | 00 | 01 | 00 |
| 48 - 61 | Not used | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | 00 | 00 | 10 | 00 |
| 63 | Checksum of Byte 0-62 | 86 | 0D | 98 | 87 |
| 64 | Manufacturer's JEDEC ID Code (1) | 7F | 7F | 7F | 7F |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Product Type | | HYS72D128300GBR-7-B | HYS72D128321GBR-7-B | HYS72D256220GBR-7-B | HYS72D256320GBR-7-B |
|--------------------|----------------------------------|---------------------|---------------------|---------------------|---------------------|
| Organization | | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2100R-20330 | PC2100R-20330 | PC2100R-20331 | PC2100R-20330 |
| JEDEC SPD Revision | | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 65 | Manufacturer's JEDEC ID Code (2) | 7F | 7F | 7F | 7F |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx | xx | xx |
| 73 | Part Number, Char 1 | 37 | 37 | 37 | 37 |
| 74 | Part Number, Char 2 | 32 | 32 | 32 | 32 |
| 75 | Part Number, Char 3 | 44 | 44 | 44 | 44 |
| 76 | Part Number, Char 4 | 31 | 31 | 32 | 32 |
| 77 | Part Number, Char 5 | 32 | 32 | 35 | 35 |
| 78 | Part Number, Char 6 | 38 | 38 | 36 | 36 |
| 79 | Part Number, Char 7 | 33 | 33 | 32 | 33 |
| 80 | Part Number, Char 8 | 30 | 32 | 32 | 32 |
| 81 | Part Number, Char 9 | 30 | 31 | 30 | 30 |
| 82 | Part Number, Char 10 | 47 | 47 | 47 | 47 |
| 83 | Part Number, Char 11 | 42 | 42 | 42 | 42 |
| 84 | Part Number, Char 12 | 52 | 52 | 52 | 52 |
| 85 | Part Number, Char 13 | 37 | 37 | 37 | 37 |
| 86 | Part Number, Char 14 | 42 | 42 | 42 | 42 |
| 87 | Part Number, Char 15 | 20 | 20 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 | 20 | 20 |
| 89 | Part Number, Char 17 | 20 | 20 | 20 | 20 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | |
|---------------------------|--------------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D128300GBR-7-B | HYS72D128321GBR-7-B | HYS72D256220GBR-7-B | HYS72D256320GBR-7-B |
| Organization | | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2100R-20330 | PC2100R-20330 | PC2100R-20331 | PC2100R-20330 |
| JEDEC SPD Revision | | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 90 | Part Number, Char 18 | 20 | 20 | 20 | 20 |
| 91 | Module Revision Code | 1x | 1x | 1x | 1x |
| 92 | Test Program Revision Code | xx | xx | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx | xx | xx |
| 99 - 127 | Not used | 00 | 00 | 00 | 00 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

TABLE 19
HYS72D[128/256]xxxHBR-5-B

| Product Type | | HYS72D64301HBR-5-B | HYS72D128300HBR-5-B | HYS72D128321HBR-5-B | HYS72D256220HBR-5-B | HYS72D256320HBR-5-B |
|--------------------|--|--------------------|---------------------|---------------------|---------------------|---------------------|
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 0 | Programmed SPD Bytes in E ² PROM | 80 | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in E ² PROM | 08 | 08 | 08 | 08 | 08 |
| 2 | Memory Type (DDR = 07h) | 07 | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 0D | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 0B | 0C | 0B | 0C | 0C |
| 5 | Number of DIMM Ranks | 01 | 01 | 02 | 02 | 02 |
| 6 | Data Width (LSB) | 48 | 48 | 48 | 48 | 48 |
| 7 | Data Width (MSB) | 00 | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 | 04 | 04 | 04 |
| 9 | t _{CK} @ CL _{max} (Byte 18) [ns] | 50 | 50 | 50 | 50 | 50 |
| 10 | t _{AC} SDRAM @ CL _{max} (Byte 18) [ns] | 50 | 50 | 50 | 50 | 50 |
| 11 | Error Correction Support | 02 | 02 | 02 | 02 | 02 |
| 12 | Refresh Rate | 82 | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM Width | 08 | 04 | 08 | 04 | 04 |
| 14 | Error Checking SDRAM Width | 08 | 04 | 08 | 04 | 04 |
| 15 | t _{CCD} [cycles] | 01 | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E | 0E | 0E | 0E |
| 17 | Number of Banks on SDRAM Device | 04 | 04 | 04 | 04 | 04 |
| 18 | CAS Latency | 1C | 1C | 1C | 1C | 1C |
| 19 | CS Latency | 01 | 01 | 01 | 01 | 01 |
| 20 | Write Latency | 02 | 02 | 02 | 02 | 02 |
| 21 | DIMM Attributes | 26 | 26 | 26 | 26 | 26 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Product Type | | HYS72D64301HBR-5-B | HYS72D128300HBR-5-B | HYS72D128321HBR-5-B | HYS72D256220HBR-5-B | HYS72D256320HBR-5-B |
|--------------------|---|--------------------|---------------------|---------------------|---------------------|---------------------|
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 22 | Component Attributes | C1 | C1 | C1 | C1 | C1 |
| 23 | t _{CK} @ CL _{max} -0.5 (Byte 18) [ns] | 60 | 60 | 60 | 60 | 60 |
| 24 | t _{AC} SDRAM @ CL _{max} -0.5 [ns] | 50 | 50 | 50 | 50 | 50 |
| 25 | t _{CK} @ CL _{max} -1 (Byte 18) [ns] | 75 | 75 | 75 | 75 | 75 |
| 26 | t _{AC} SDRAM @ CL _{max} -1 [ns] | 50 | 50 | 50 | 50 | 50 |
| 27 | t _{RPmin} [ns] | 3C | 3C | 3C | 3C | 3C |
| 28 | t _{RRDmin} [ns] | 28 | 28 | 28 | 28 | 28 |
| 29 | t _{RCDmin} [ns] | 3C | 3C | 3C | 3C | 3C |
| 30 | t _{RASmin} [ns] | 28 | 28 | 28 | 28 | 28 |
| 31 | Module Density per Rank | 80 | 01 | 80 | 01 | 01 |
| 32 | t _{AS} , t _{CS} [ns] | 60 | 60 | 60 | 60 | 60 |
| 33 | t _{AH} , t _{CH} [ns] | 60 | 60 | 60 | 60 | 60 |
| 34 | t _{DS} [ns] | 40 | 40 | 40 | 40 | 40 |
| 35 | t _{DH} [ns] | 40 | 40 | 40 | 40 | 40 |
| 36 - 40 | Not used | 00 | 00 | 00 | 00 | 00 |
| 41 | t _{RCmin} [ns] | 37 | 37 | 37 | 37 | 37 |
| 42 | t _{RFCmin} [ns] | 41 | 41 | 41 | 41 | 41 |
| 43 | t _{CKmax} [ns] | 28 | 28 | 28 | 28 | 28 |
| 44 | t _{DQSQmax} [ns] | 28 | 28 | 28 | 28 | 28 |
| 45 | t _{QHSmax} [ns] | 50 | 50 | 50 | 50 | 50 |
| 46 | not used | 00 | 00 | 00 | 00 | 00 |
| 47 | DIMM PCB Height | 01 | 01 | 01 | 01 | 01 |
| 48 - 61 | Not used | 00 | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | 10 | 10 | 10 | 10 | 10 |
| 63 | Checksum of Byte 0-62 | 67 | E1 | 68 | E2 | E2 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | | |
|---------------------------|----------------------------------|---------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D64301HBR-5-B | HYS72D128300HBR-5-B | HYS72D128321HBR-5-B | HYS72D256220HBR-5-B | HYS72D256320HBR-5-B |
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 64 | Manufacturer's JEDEC ID Code (1) | 7F | 7F | 7F | 7F | 7F |
| 65 | Manufacturer's JEDEC ID Code (2) | 7F | 7F | 7F | 7F | 7F |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F | 7F | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F | 7F | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F | 7F | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 | 51 | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 | 00 | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 | 00 | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx | xx | xx | xx |
| 73 | Part Number, Char 1 | 37 | 37 | 37 | 37 | 37 |
| 74 | Part Number, Char 2 | 32 | 32 | 32 | 32 | 32 |
| 75 | Part Number, Char 3 | 44 | 44 | 44 | 44 | 44 |
| 76 | Part Number, Char 4 | 36 | 31 | 31 | 32 | 32 |
| 77 | Part Number, Char 5 | 34 | 32 | 32 | 35 | 35 |
| 78 | Part Number, Char 6 | 33 | 38 | 38 | 36 | 36 |
| 79 | Part Number, Char 7 | 30 | 33 | 33 | 32 | 33 |
| 80 | Part Number, Char 8 | 31 | 30 | 32 | 32 | 32 |
| 81 | Part Number, Char 9 | 48 | 30 | 31 | 30 | 30 |
| 82 | Part Number, Char 10 | 42 | 48 | 48 | 48 | 48 |
| 83 | Part Number, Char 11 | 52 | 42 | 42 | 42 | 42 |
| 84 | Part Number, Char 12 | 35 | 52 | 52 | 52 | 52 |
| 85 | Part Number, Char 13 | 42 | 35 | 35 | 35 | 35 |
| 86 | Part Number, Char 14 | 20 | 42 | 42 | 42 | 42 |
| 87 | Part Number, Char 15 | 20 | 20 | 20 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 | 20 | 20 | 20 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | | |
|---------------------------|--------------------------------|---------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D64301HBR-5-B | HYS72D128300HBR-5-B | HYS72D128321HBR-5-B | HYS72D256220HBR-5-B | HYS72D256320HBR-5-B |
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 | PC3200R-30331 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 | Rev. 1.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 89 | Part Number, Char 17 | 20 | 20 | 20 | 20 | 20 |
| 90 | Part Number, Char 18 | 20 | 20 | 20 | 20 | 20 |
| 91 | Module Revision Code | 1x | 1x | 1x | 1x | 1x |
| 92 | Test Program Revision Code | xx | xx | xx | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx | xx | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx | xx | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx | xx | xx | xx |
| 99 - 127 | Not used | 00 | 00 | 00 | 00 | 00 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

TABLE 20
HYS72D[128/256]xxxHBR-6-B

| Product Type | | HYS72D64301HBR-6-B | HYS72D128300HBR-6-B | HYS72D128321HBR-6-B | HYS72D256220HBR-6-B | HYS72D256320HBR-6-B |
|--------------------|--|--------------------|---------------------|---------------------|---------------------|---------------------|
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2700R-25331 | PC2700R-25330 | PC2700R-25330 | PC2700R-25331 | PC2700R-25330 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 0 | Programmed SPD Bytes in E ² PROM | 80 | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in E ² PROM | 08 | 08 | 08 | 08 | 08 |
| 2 | Memory Type (DDR = 07h) | 07 | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 0D | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 0B | 0C | 0B | 0C | 0C |
| 5 | Number of DIMM Ranks | 01 | 01 | 02 | 02 | 02 |
| 6 | Data Width (LSB) | 48 | 48 | 48 | 48 | 48 |
| 7 | Data Width (MSB) | 00 | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 | 04 | 04 | 04 |
| 9 | t _{CK} @ CL _{max} (Byte 18) [ns] | 60 | 60 | 60 | 60 | 60 |
| 10 | t _{AC} SDRAM @ CL _{max} (Byte 18) [ns] | 70 | 70 | 70 | 70 | 70 |
| 11 | Error Correction Support | 02 | 02 | 02 | 02 | 02 |
| 12 | Refresh Rate | 82 | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM Width | 08 | 04 | 08 | 04 | 04 |
| 14 | Error Checking SDRAM Width | 08 | 04 | 08 | 04 | 04 |
| 15 | t _{CCD} [cycles] | 01 | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E | 0E | 0E | 0E |
| 17 | Number of Banks on SDRAM Device | 04 | 04 | 04 | 04 | 04 |
| 18 | CAS Latency | 0C | 0C | 0C | 0C | 0C |
| 19 | CS Latency | 01 | 01 | 01 | 01 | 01 |
| 20 | Write Latency | 02 | 02 | 02 | 02 | 02 |
| 21 | DIMM Attributes | 26 | 26 | 26 | 26 | 26 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Product Type | | HYS72D64301HBR-6-B | HYS72D128300HBR-6-B | HYS72D128321HBR-6-B | HYS72D256220HBR-6-B | HYS72D256320HBR-6-B |
|--------------------|---|--------------------|---------------------|---------------------|---------------------|---------------------|
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2700R-25331 | PC2700R-25330 | PC2700R-25330 | PC2700R-25331 | PC2700R-25330 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 22 | Component Attributes | C1 | C1 | C1 | C1 | C1 |
| 23 | t _{CK} @ CL _{max} -0.5 (Byte 18) [ns] | 75 | 75 | 75 | 75 | 75 |
| 24 | t _{AC} SDRAM @ CL _{max} -0.5 [ns] | 70 | 70 | 70 | 70 | 70 |
| 25 | t _{CK} @ CL _{max} -1 (Byte 18) [ns] | 00 | 00 | 00 | 00 | 00 |
| 26 | t _{AC} SDRAM @ CL _{max} -1 [ns] | 00 | 00 | 00 | 00 | 00 |
| 27 | t _{RPmin} [ns] | 48 | 48 | 48 | 48 | 48 |
| 28 | t _{RRDmin} [ns] | 30 | 30 | 30 | 30 | 30 |
| 29 | t _{RCDmin} [ns] | 48 | 48 | 48 | 48 | 48 |
| 30 | t _{RASmin} [ns] | 2A | 2A | 2A | 2A | 2A |
| 31 | Module Density per Rank | 80 | 01 | 80 | 01 | 01 |
| 32 | t _{AS} , t _{CS} [ns] | 75 | 75 | 75 | 75 | 75 |
| 33 | t _{AH} , t _{CH} [ns] | 75 | 75 | 75 | 75 | 75 |
| 34 | t _{DS} [ns] | 45 | 45 | 45 | 45 | 45 |
| 35 | t _{DH} [ns] | 45 | 45 | 45 | 45 | 45 |
| 36 - 40 | Not used | 00 | 00 | 00 | 00 | 00 |
| 41 | t _{RCmin} [ns] | 3C | 3C | 3C | 3C | 3C |
| 42 | t _{RFCmin} [ns] | 48 | 48 | 48 | 48 | 48 |
| 43 | t _{CKmax} [ns] | 30 | 30 | 30 | 30 | 30 |
| 44 | t _{DQSQmax} [ns] | 28 | 28 | 28 | 28 | 28 |
| 45 | t _{QHSmax} [ns] | 50 | 50 | 50 | 50 | 50 |
| 46 | not used | 00 | 00 | 00 | 00 | 00 |
| 47 | DIMM PCB Height | 01 | 00 | 00 | 01 | 00 |
| 48 - 61 | Not used | 00 | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | 10 | 00 | 00 | 10 | 00 |
| 63 | Checksum of Byte 0-62 | 61 | CA | 51 | DC | CB |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | | |
|---------------------------|----------------------------------|---------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D64301HBR-6-B | HYS72D128300HBR-6-B | HYS72D128321HBR-6-B | HYS72D256220HBR-6-B | HYS72D256320HBR-6-B |
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2700R-25331 | PC2700R-25330 | PC2700R-25330 | PC2700R-25331 | PC2700R-25330 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 64 | Manufacturer's JEDEC ID Code (1) | 7F | 7F | 7F | 7F | 7F |
| 65 | Manufacturer's JEDEC ID Code (2) | 7F | 7F | 7F | 7F | 7F |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F | 7F | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F | 7F | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F | 7F | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 | 51 | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 | 00 | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 | 00 | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx | xx | xx | xx |
| 73 | Part Number, Char 1 | 37 | 37 | 37 | 37 | 37 |
| 74 | Part Number, Char 2 | 32 | 32 | 32 | 32 | 32 |
| 75 | Part Number, Char 3 | 44 | 44 | 44 | 44 | 44 |
| 76 | Part Number, Char 4 | 36 | 31 | 31 | 32 | 32 |
| 77 | Part Number, Char 5 | 34 | 32 | 32 | 35 | 35 |
| 78 | Part Number, Char 6 | 33 | 38 | 38 | 36 | 36 |
| 79 | Part Number, Char 7 | 30 | 33 | 33 | 32 | 33 |
| 80 | Part Number, Char 8 | 31 | 30 | 32 | 32 | 32 |
| 81 | Part Number, Char 9 | 48 | 30 | 31 | 30 | 30 |
| 82 | Part Number, Char 10 | 42 | 48 | 48 | 48 | 48 |
| 83 | Part Number, Char 11 | 52 | 42 | 42 | 42 | 42 |
| 84 | Part Number, Char 12 | 36 | 52 | 52 | 52 | 52 |
| 85 | Part Number, Char 13 | 42 | 36 | 36 | 36 | 36 |
| 86 | Part Number, Char 14 | 20 | 42 | 42 | 42 | 42 |
| 87 | Part Number, Char 15 | 20 | 20 | 20 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 | 20 | 20 | 20 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | | |
|---------------------------|--------------------------------|---------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D64301HBR-6-B | HYS72D128300HBR-6-B | HYS72D128321HBR-6-B | HYS72D256220HBR-6-B | HYS72D256320HBR-6-B |
| Organization | | 512MB | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×8) | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2700R -25331 | PC2700R -25330 | PC2700R -25330 | PC2700R -25331 | PC2700R -25330 |
| JEDEC SPD Revision | | Rev. 1.0 | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX | HEX |
| 89 | Part Number, Char 17 | 20 | 20 | 20 | 20 | 20 |
| 90 | Part Number, Char 18 | 20 | 20 | 20 | 20 | 20 |
| 91 | Module Revision Code | 1x | 1x | 1x | 1x | 1x |
| 92 | Test Program Revision Code | xx | xx | xx | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx | xx | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx | xx | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx | xx | xx | xx |
| 99 - 127 | Not used | 00 | 00 | 00 | 00 | 00 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

TABLE 21
HYS72D[128/256]xxxHBR-7-B

| Product Type | | HYS72D128300HBR-7-B | HYS72D128321HBR-7-B | HYS72D256220HBR-7-B | HYS72D256320HBR-7-B |
|--------------------|--|---------------------|---------------------|---------------------|---------------------|
| Organization | | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2100R-20330 | PC2100R-20330 | PC2100R-20331 | PC2100R-20330 |
| JEDEC SPD Revision | | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 0 | Programmed SPD Bytes in E ² PROM | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in E ² PROM | 08 | 08 | 08 | 08 |
| 2 | Memory Type (DDR = 07h) | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 0C | 0B | 0C | 0C |
| 5 | Number of DIMM Ranks | 01 | 02 | 02 | 02 |
| 6 | Data Width (LSB) | 48 | 48 | 48 | 48 |
| 7 | Data Width (MSB) | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Levels | 04 | 04 | 04 | 04 |
| 9 | t _{CK} @ CL _{max} (Byte 18) [ns] | 70 | 70 | 70 | 70 |
| 10 | t _{AC} SDRAM @ CL _{max} (Byte 18) [ns] | 75 | 75 | 75 | 75 |
| 11 | Error Correction Support | 02 | 02 | 02 | 02 |
| 12 | Refresh Rate | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM Width | 04 | 08 | 04 | 04 |
| 14 | Error Checking SDRAM Width | 04 | 08 | 04 | 04 |
| 15 | t _{CCD} [cycles] | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 0E | 0E | 0E | 0E |
| 17 | Number of Banks on SDRAM Device | 04 | 04 | 04 | 04 |
| 18 | CAS Latency | 0C | 0C | 0C | 0C |
| 19 | CS Latency | 01 | 01 | 01 | 01 |
| 20 | Write Latency | 02 | 02 | 02 | 02 |
| 21 | DIMM Attributes | 26 | 26 | 26 | 26 |
| 22 | Component Attributes | C1 | C1 | C1 | C1 |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| Product Type | | HYS72D128300HBR-7-B | HYS72D128321HBR-7-B | HYS72D256220HBR-7-B | HYS72D256320HBR-7-B |
|--------------------|---|---------------------|---------------------|---------------------|---------------------|
| Organization | | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2100R-20330 | PC2100R-20330 | PC2100R-20331 | PC2100R-20330 |
| JEDEC SPD Revision | | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 23 | t _{CK} @ CL _{max} -0.5 (Byte 18) [ns] | 75 | 75 | 75 | 75 |
| 24 | t _{AC} SDRAM @ CL _{max} -0.5 [ns] | 75 | 75 | 75 | 75 |
| 25 | t _{CK} @ CL _{max} -1 (Byte 18) [ns] | 00 | 00 | 00 | 00 |
| 26 | t _{AC} SDRAM @ CL _{max} -1 [ns] | 00 | 00 | 00 | 00 |
| 27 | t _{RPmin} [ns] | 50 | 50 | 50 | 50 |
| 28 | t _{RRDmin} [ns] | 3C | 3C | 3C | 3C |
| 29 | t _{RCDmin} [ns] | 50 | 50 | 50 | 50 |
| 30 | t _{RASmin} [ns] | 2D | 2D | 2D | 2D |
| 31 | Module Density per Rank | 01 | 80 | 01 | 01 |
| 32 | t _{AS} , t _{CS} [ns] | 90 | 90 | 90 | 90 |
| 33 | t _{AH} , t _{CH} [ns] | 90 | 90 | 90 | 90 |
| 34 | t _{DS} [ns] | 50 | 50 | 50 | 50 |
| 35 | t _{DH} [ns] | 50 | 50 | 50 | 50 |
| 36 - 40 | Not used | 00 | 00 | 00 | 00 |
| 41 | t _{RCmin} [ns] | 41 | 41 | 41 | 41 |
| 42 | t _{RFCmin} [ns] | 4B | 4B | 4B | 4B |
| 43 | t _{CKmax} [ns] | 30 | 30 | 30 | 30 |
| 44 | t _{DQSQmax} [ns] | 32 | 32 | 32 | 32 |
| 45 | t _{QHSmax} [ns] | 75 | 75 | 75 | 75 |
| 46 | not used | 00 | 00 | 00 | 00 |
| 47 | DIMM PCB Height | 00 | 00 | 01 | 00 |
| 48 - 61 | Not used | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | 00 | 00 | 10 | 00 |
| 63 | Checksum of Byte 0-62 | 86 | 0D | 98 | 87 |
| 64 | Manufacturer's JEDEC ID Code (1) | 7F | 7F | 7F | 7F |
| 65 | Manufacturer's JEDEC ID Code (2) | 7F | 7F | 7F | 7F |



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | |
|---------------------------|----------------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D128300HBR-7-B | HYS72D128321HBR-7-B | HYS72D256220HBR-7-B | HYS72D256320HBR-7-B |
| Organization | | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2100R-20330 | PC2100R-20330 | PC2100R-20331 | PC2100R-20330 |
| JEDEC SPD Revision | | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx | xx | xx |
| 73 | Part Number, Char 1 | 37 | 37 | 37 | 37 |
| 74 | Part Number, Char 2 | 32 | 32 | 32 | 32 |
| 75 | Part Number, Char 3 | 44 | 44 | 44 | 44 |
| 76 | Part Number, Char 4 | 31 | 31 | 32 | 32 |
| 77 | Part Number, Char 5 | 32 | 32 | 35 | 35 |
| 78 | Part Number, Char 6 | 38 | 38 | 36 | 36 |
| 79 | Part Number, Char 7 | 33 | 33 | 32 | 33 |
| 80 | Part Number, Char 8 | 30 | 32 | 32 | 32 |
| 81 | Part Number, Char 9 | 30 | 31 | 30 | 30 |
| 82 | Part Number, Char 10 | 48 | 48 | 48 | 48 |
| 83 | Part Number, Char 11 | 42 | 42 | 42 | 42 |
| 84 | Part Number, Char 12 | 52 | 52 | 52 | 52 |
| 85 | Part Number, Char 13 | 37 | 37 | 37 | 37 |
| 86 | Part Number, Char 14 | 42 | 42 | 42 | 42 |
| 87 | Part Number, Char 15 | 20 | 20 | 20 | 20 |
| 88 | Part Number, Char 16 | 20 | 20 | 20 | 20 |
| 89 | Part Number, Char 17 | 20 | 20 | 20 | 20 |
| 90 | Part Number, Char 18 | 20 | 20 | 20 | 20 |
| 91 | Module Revision Code | 1x | 1x | 1x | 1x |



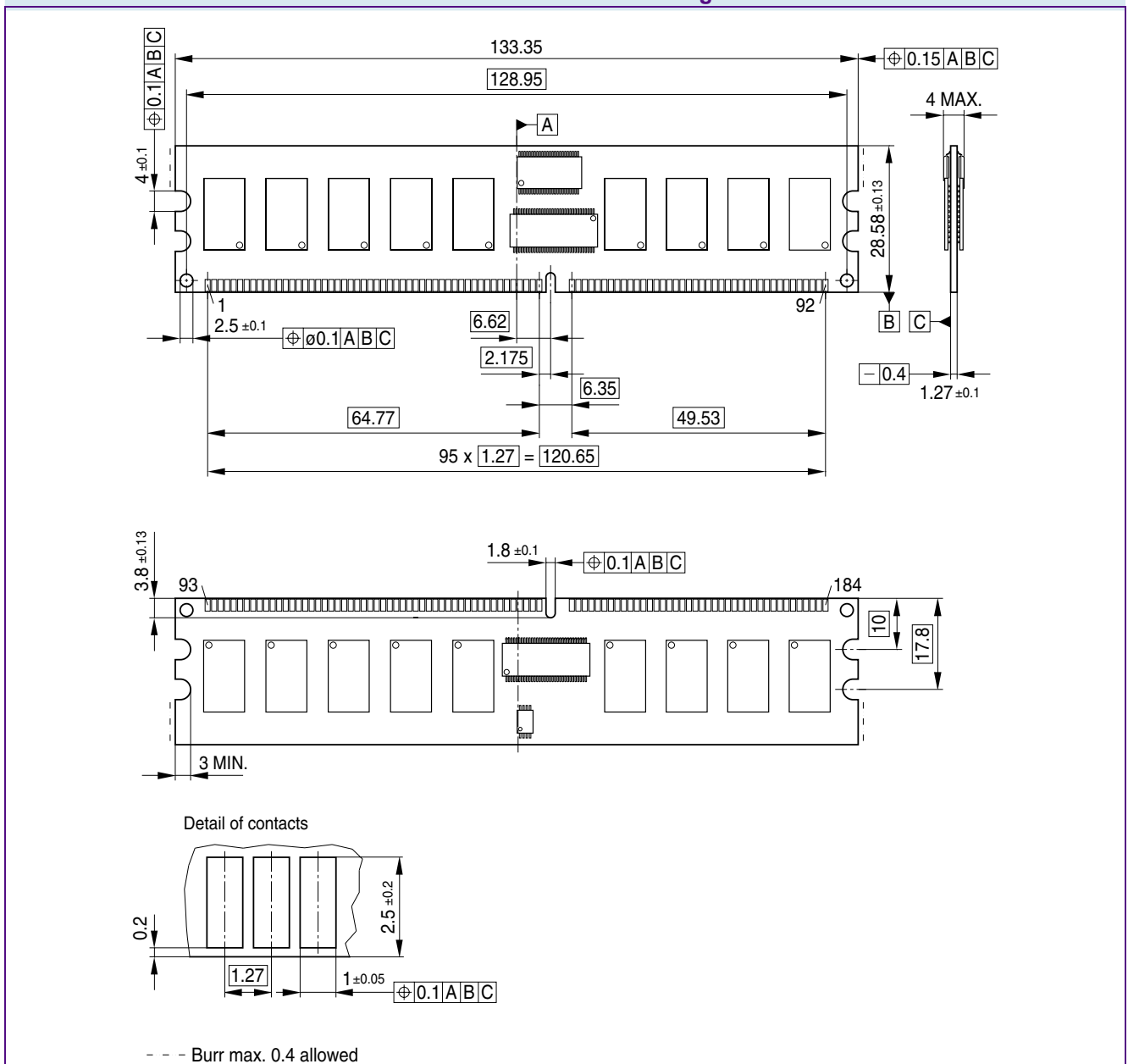
HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

| | | | | | |
|---------------------------|--------------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Product Type | | HYS72D128300HBR-7-B | HYS72D128321HBR-7-B | HYS72D256220HBR-7-B | HYS72D256320HBR-7-B |
| Organization | | 1 GByte | 1 GByte | 2 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 2 Ranks (×8) | 2 Ranks (×4) | 2 Ranks (×4) |
| Label Code | | PC2100R-20330 | PC2100R-20330 | PC2100R-20331 | PC2100R-20330 |
| JEDEC SPD Revision | | Rev. 0.0 | Rev. 0.0 | Rev. 1.0 | Rev. 0.0 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 92 | Test Program Revision Code | xx | xx | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx | xx | xx |
| 99 - 127 | Not used | 00 | 00 | 00 | 00 |



5 Package Outline

FIGURE 2
Package Outline Raw Card C - L-DIM-184-22-2



Notes

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15



HYS72D[64/128/256]xxx[G/H]BR-[5/6/7]-B
Registered DDR SDRAM Module

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